



A785GM-M7

Rev:2.0

SCHEMATICS TABLE:

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REVISION HISTORY:

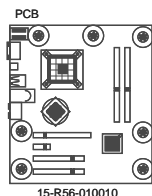
Rev	Date	Notes
A	2009-09-04	INITIAL RELEASE Change from A785GM-M5 V:A 1.Delete LPT and IR. 2.Add one front USB header F_USB3. 3.Change the USB connector power. 4.Add CPU Over Clocking circuit. 5.Add UP6262 for CPU and NB to enhance the voltage. 6.VRM chipset change RT8855 to RT8861. 7.Change to support AM3 CPU and DDR3. 8.Add a HDMI connector.
1.0	2009-11-06	1.Modify CPU VRM circuit according to the manufacturer's recommendations. 2.Modify VCC_DUAL power.
2.0	2010-01-06	1.Modify CPU VRM circuit RT8861 Colay RT8855.

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example 1) DESIGN NOTES in text for the design note to grey are information notes.
show the note inside the colored box.

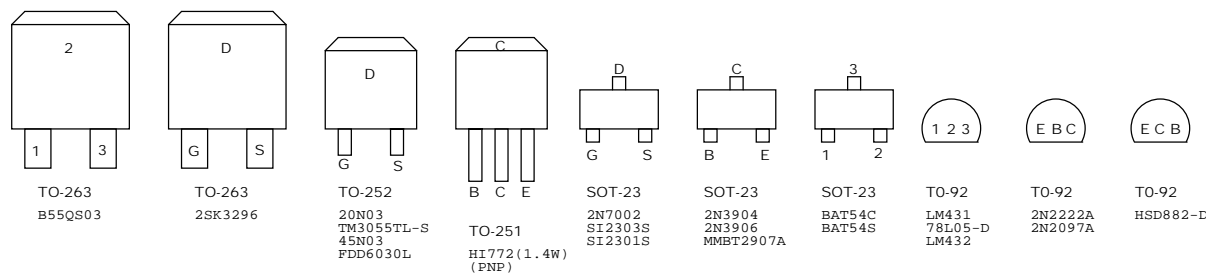
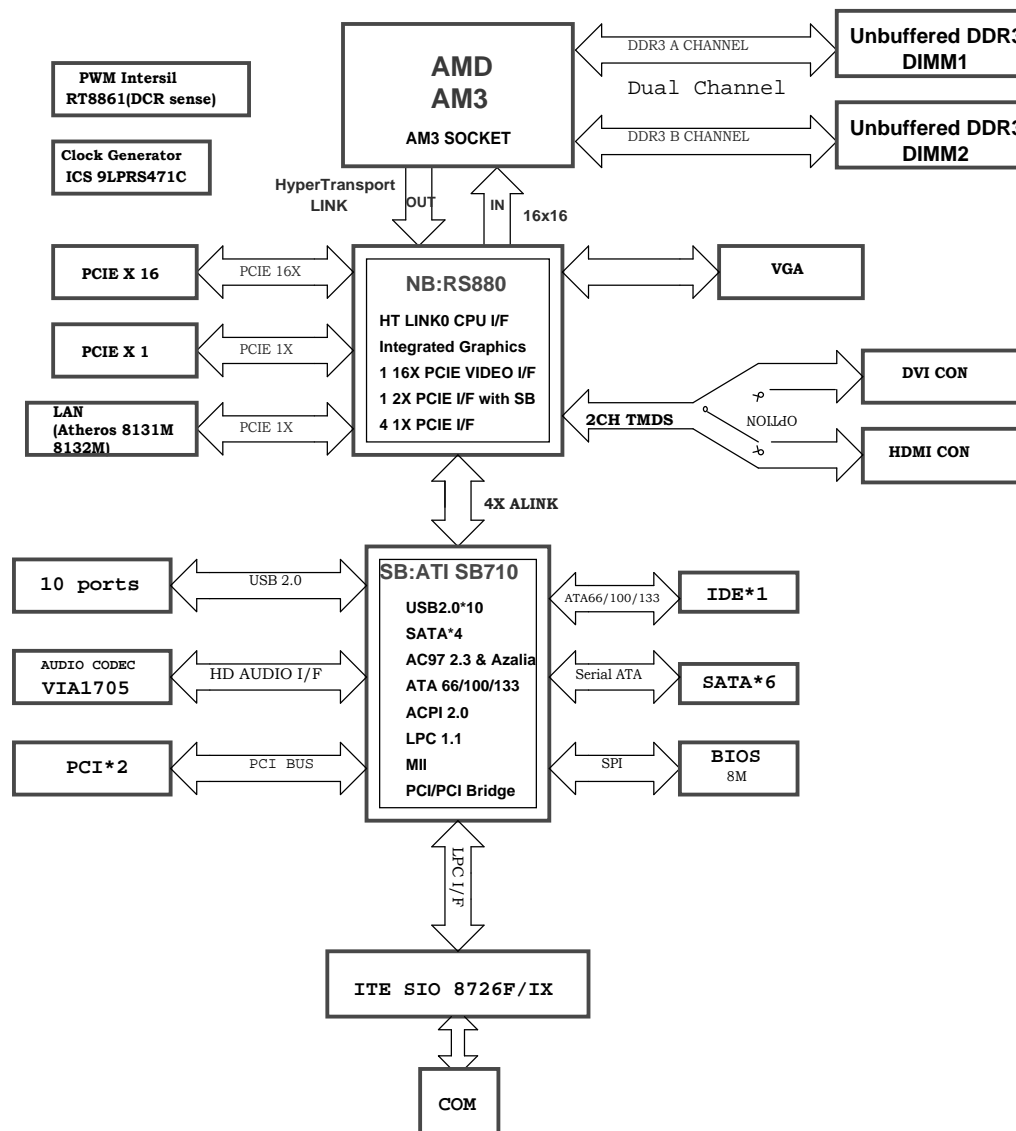
DESIGN NOTE: Example 2) DESIGN NOTES in text for the design note to yellow are notes of caution.
show the note inside the colored box.

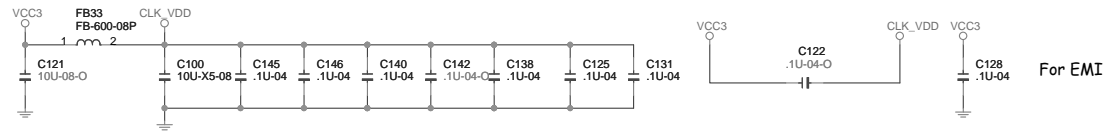
DESIGN NOTE: Example 3) DESIGN NOTES in red are critical, and must be understood and followed.



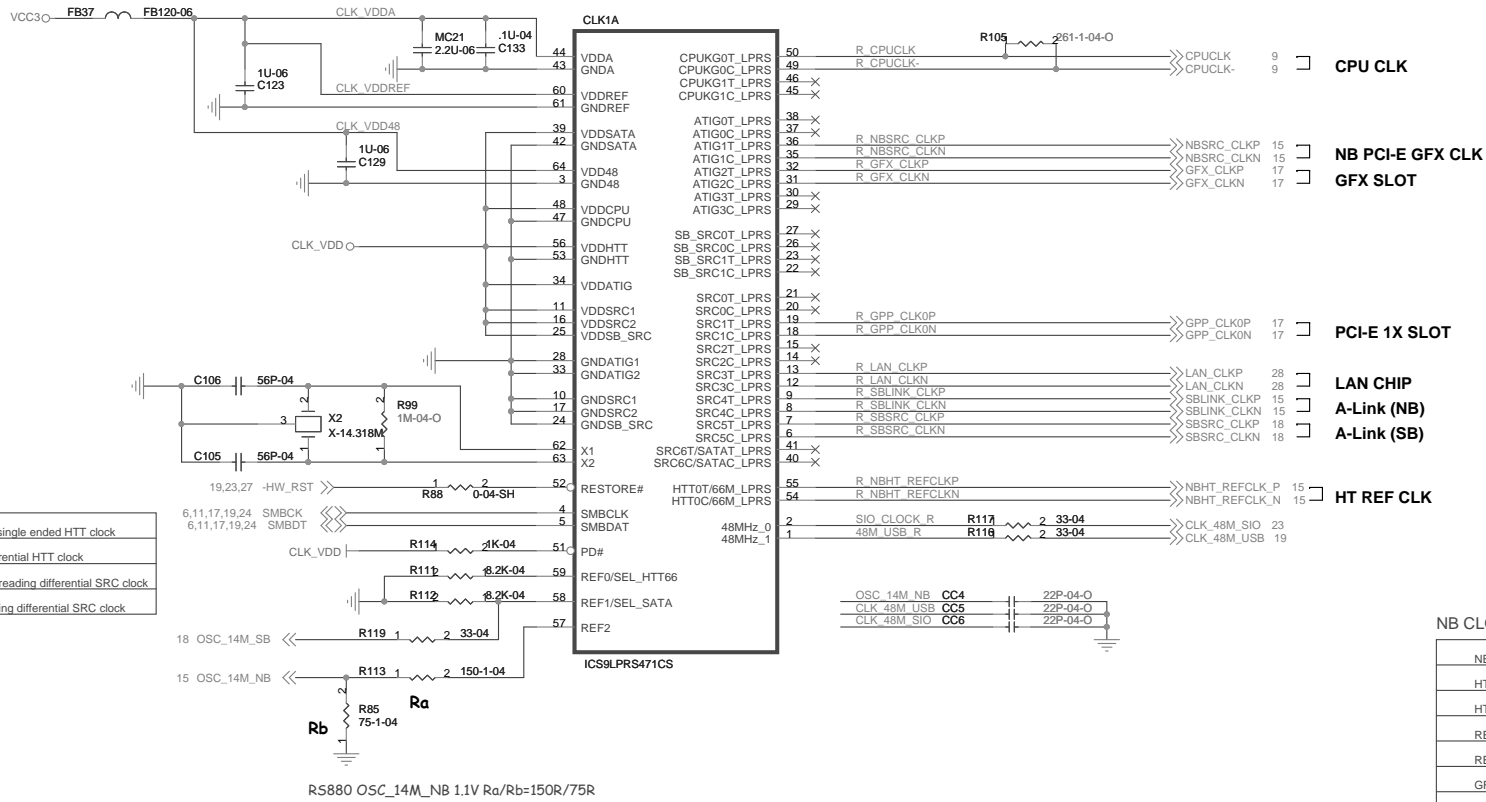
PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

		Elitegroup Computer Systems	
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- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO CLOCK GEN
- 2- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock

* default

NB CLOCK INPUT TABLE

NB CLOCKS	RS880
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	VREF
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

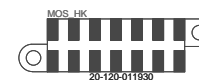
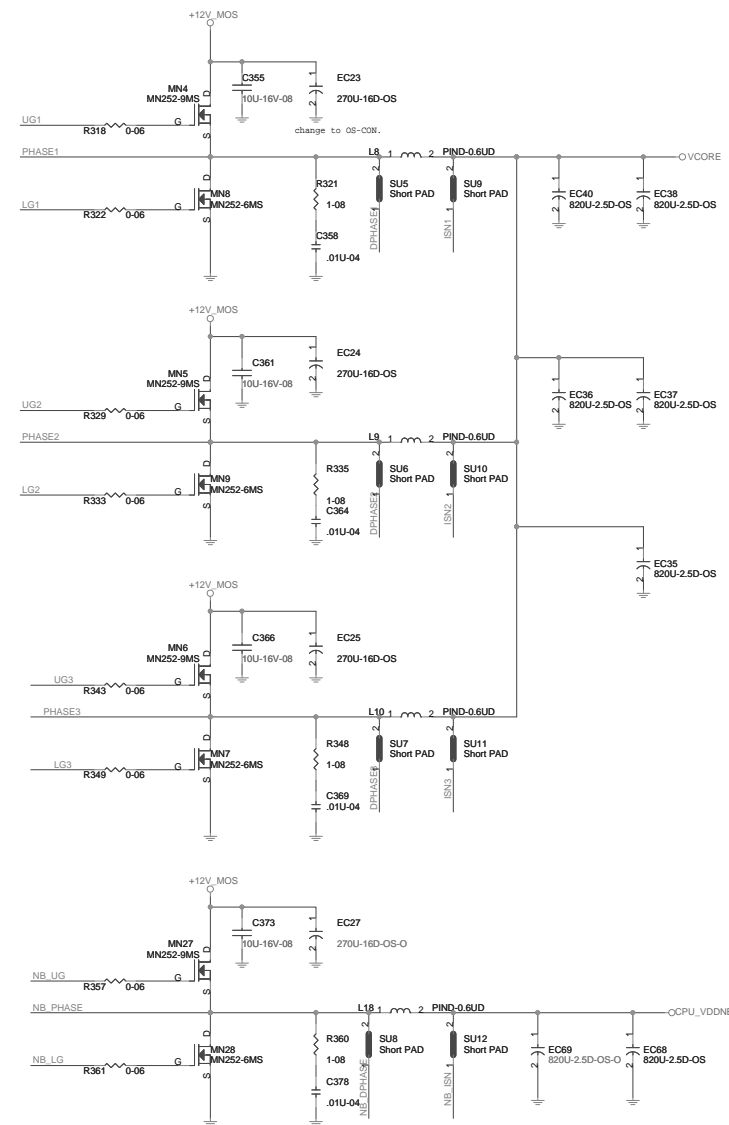
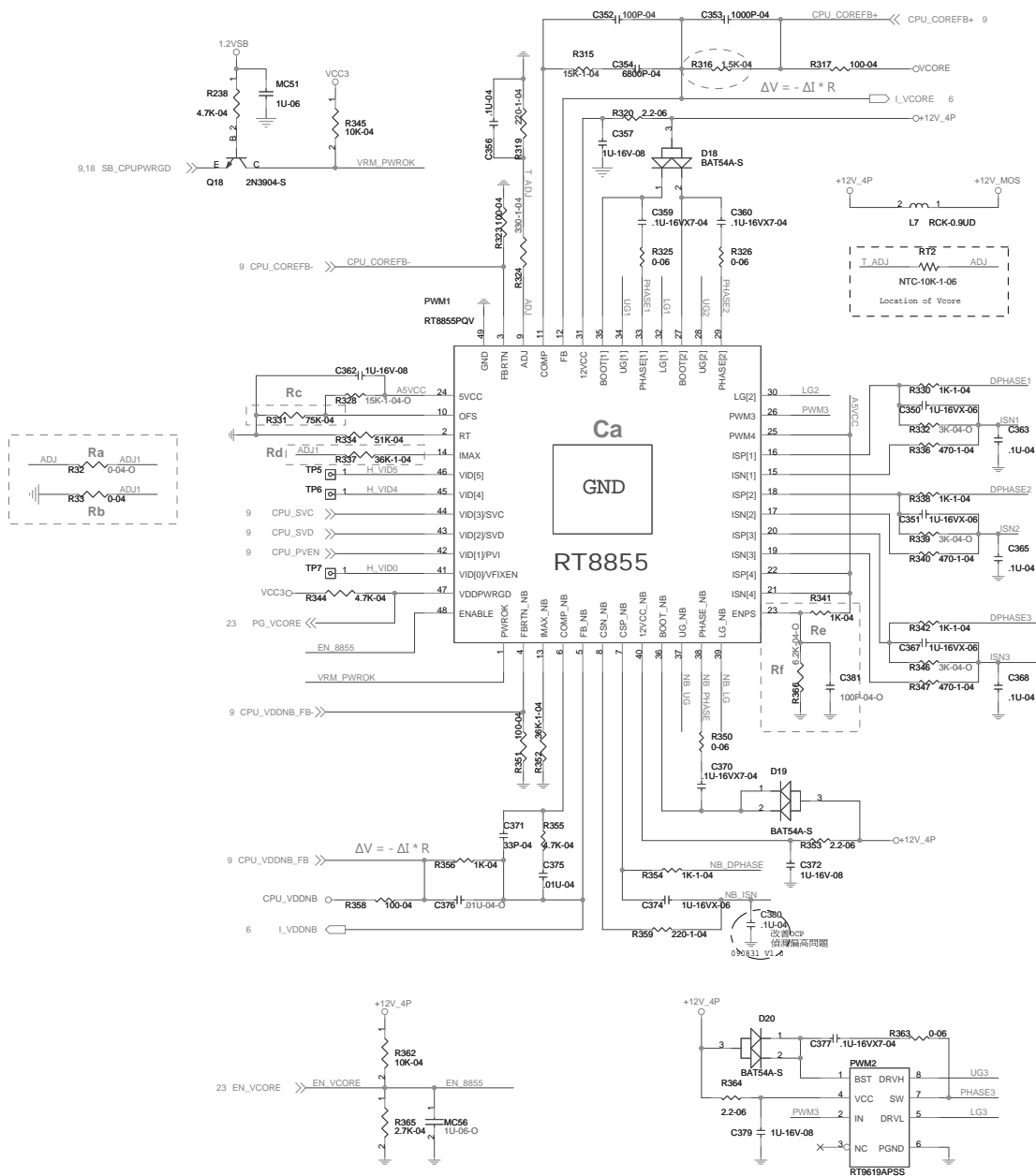
* RS880 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.
Clock chip has internal serial terminations for differential pairs

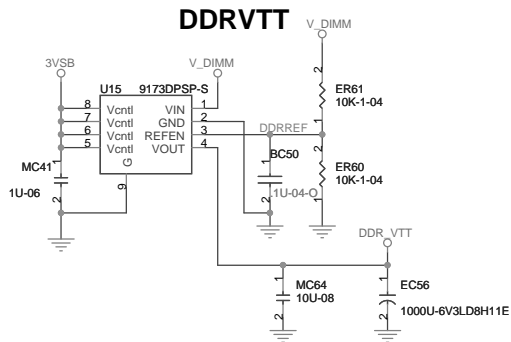
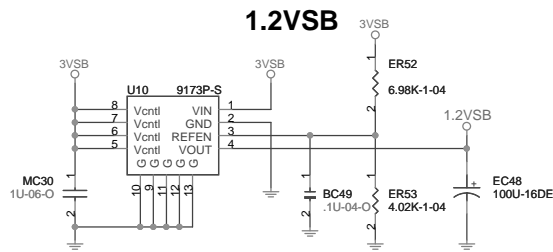
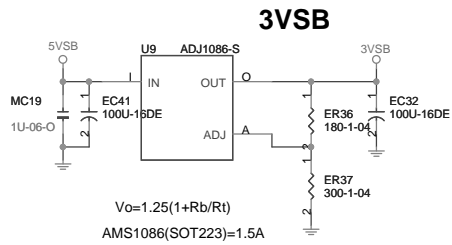
ECS Elitegroup Computer Systems

Title			
Clock Generator			
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Offset

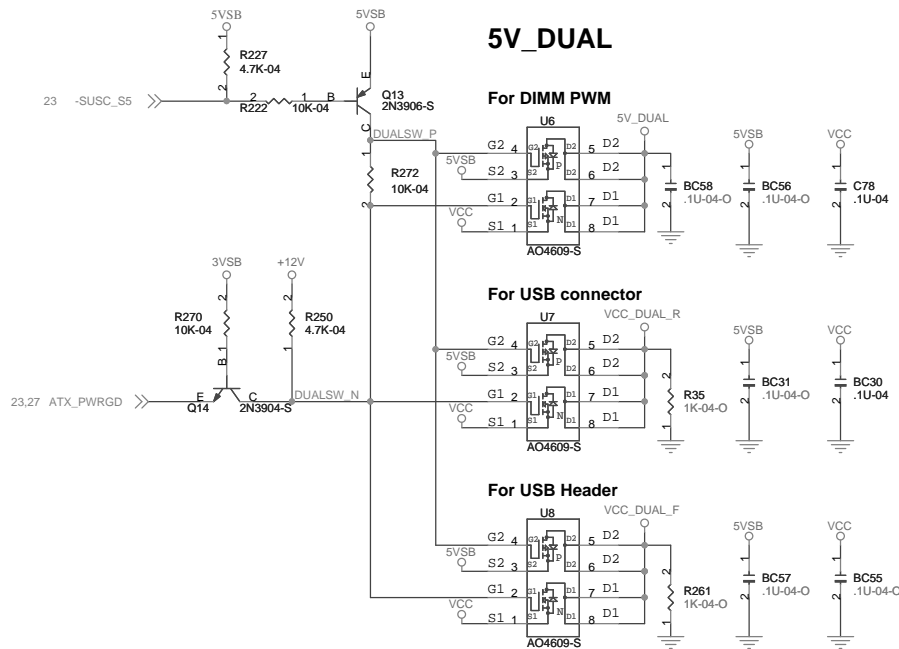
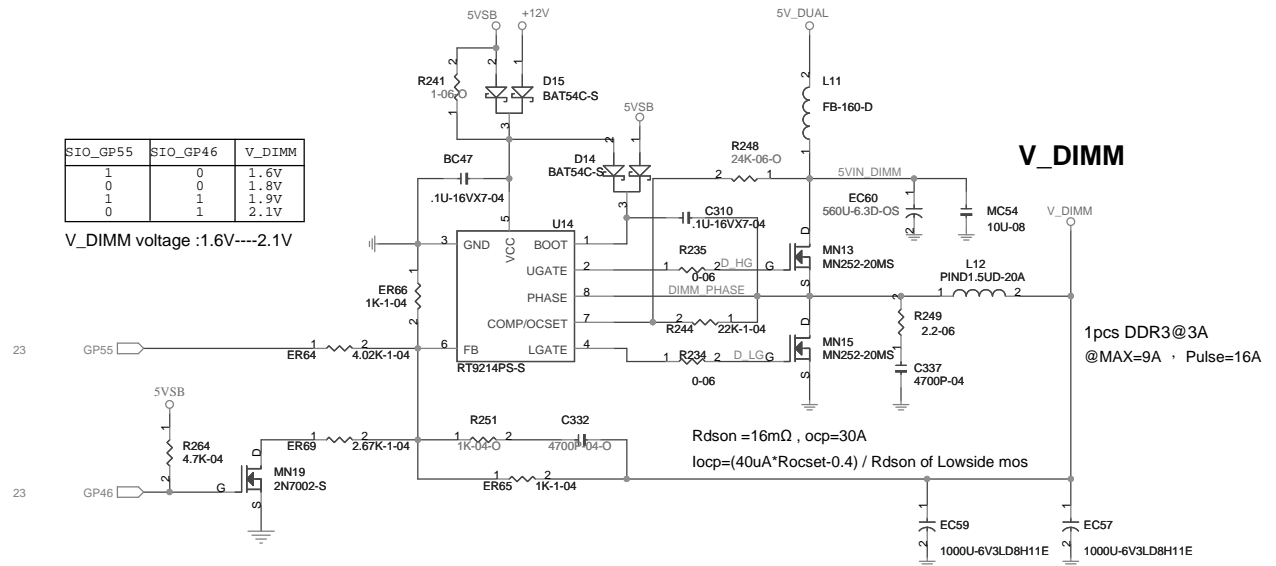
Location	Ca	Ra	Rb	Rc	Rd	Re	Rf
RT8855	RT8855	NC	0-04	75K-04	36K-1-04	1K-04	NC
RT8861	RT8861	0-04	NC	75K-04	12K-1-04	30K-1-04	6.2K-04



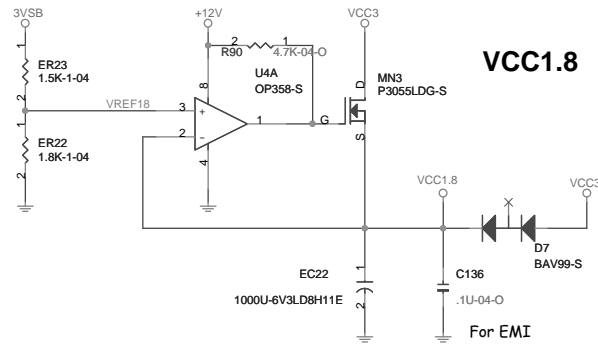


SIO_GP55	SIO_GP46	V_DIMM
1	0	1.6V
0	0	1.8V
1	1	1.9V
0	1	2.1V

V_DIMM voltage :1.6V----2.1V

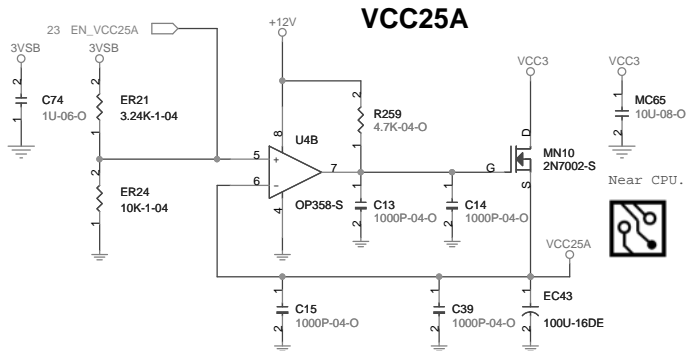


	S5	enter	S0	enter	S3	exit	S3	enter	S5	S5
-SUSC_S5	0	0	1	1	1	1	1	0	0	0
ATX_PWRGD	0	1	1	0	1	1	1	0	0	0
DUALSW_P	5VSB	5VSB	12V	0	12V	5VSB	5VSB	5VSB	5VSB	5VSB
DUALSW_N	0	12V	12V	0	12V	12V	12V	0	0	0
5V_DUAL	X	VCC5	VCC5	5VSB	VCC5	VCC5	VCC5	0	0	0
VDIMM	X	V	V	V	V	V	V	V	V	X



VCC1.8

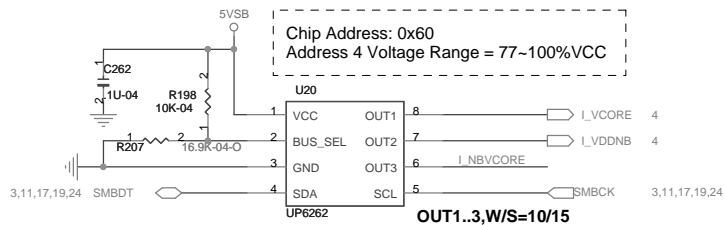
For EMI



VCC25A

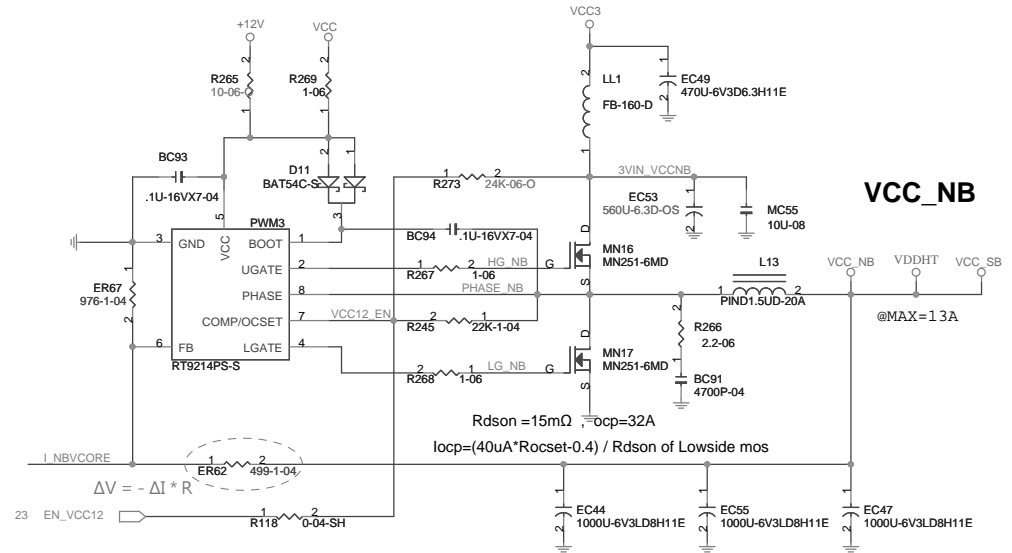
Near CPU.

uP6262的電流輸出與 ΔV_{out} 的關係如下:
選取從uP6262輸出的方向為正,
則VCORE,VCC_NB及VDIMM的 ΔV_{out} 為:
 $\Delta V_{out} = -I_c * R_{FB}$;



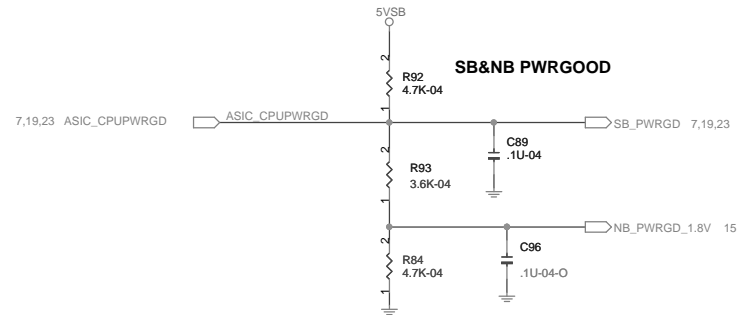
Chip Address: 0x60
Address 4 Voltage Range = 77~100%VCC

OUT1..3,W/S=10/15



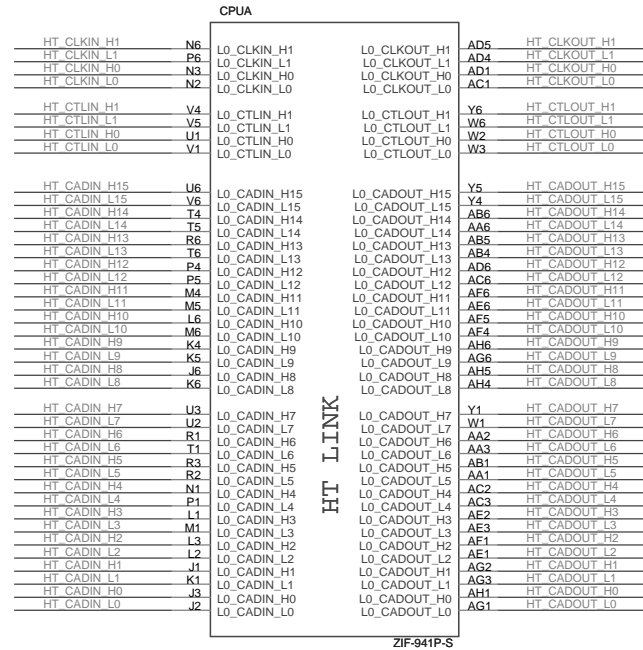
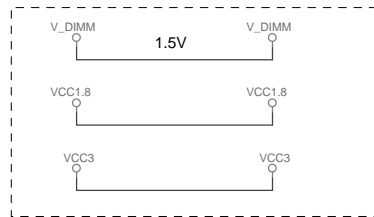
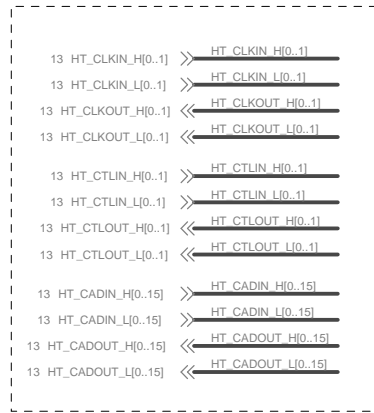
VCC_NB

HW default :VCC_NB = 1.2V

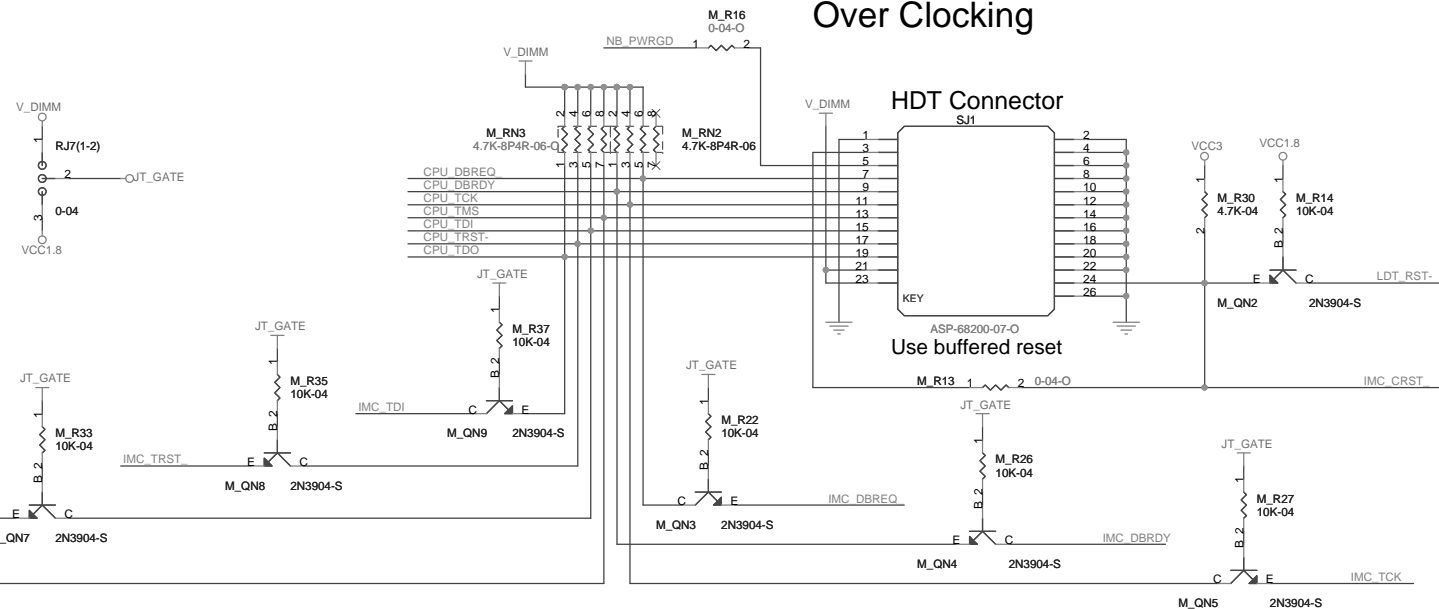
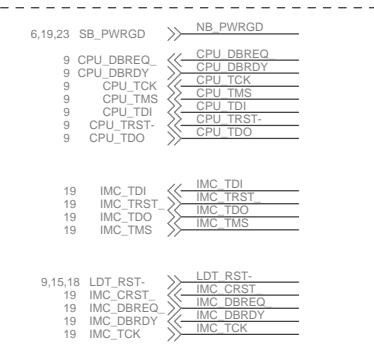
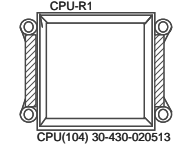
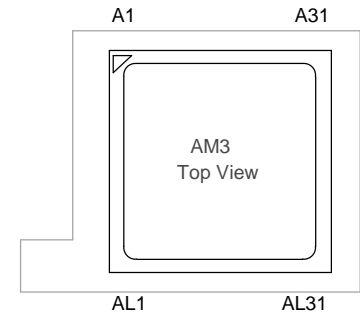


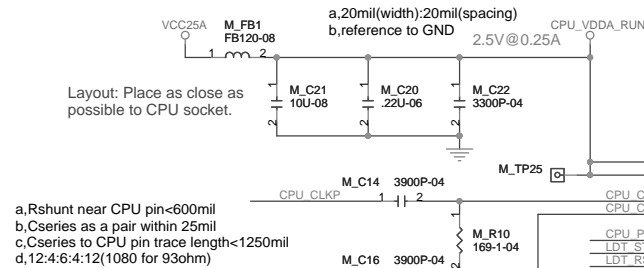
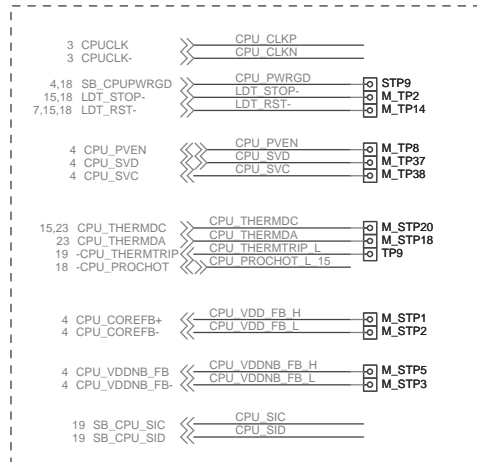
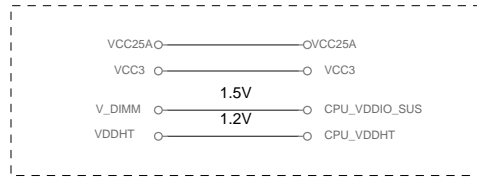
SB&NB PWRGOOD

HyperTransport

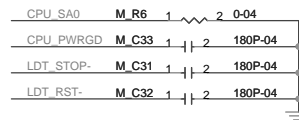
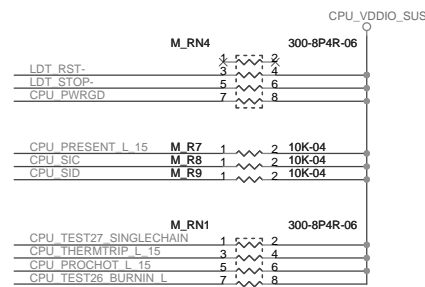
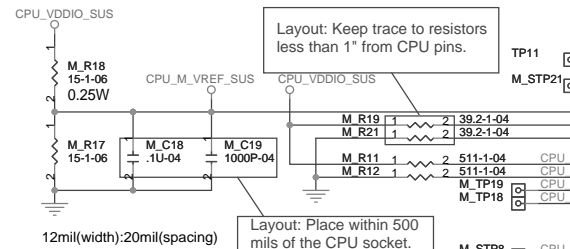


Please use 1mm pad size,
 place all ELT test pads
 on bottom side only.



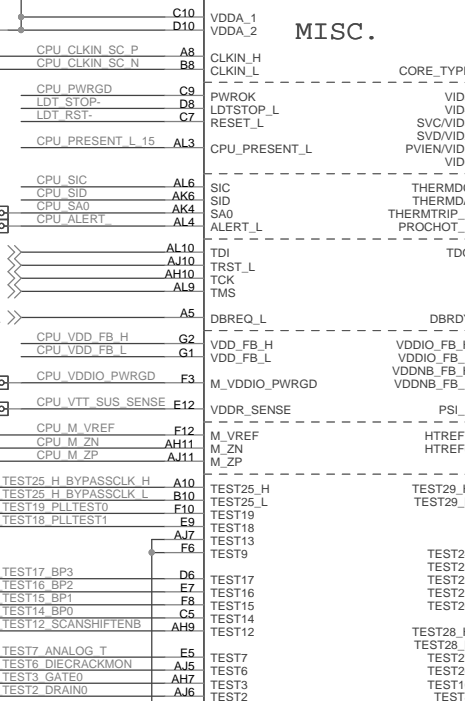


a,Rshunt near CPU pin<600mil
b,Cseries as a pair within 25mil
c,Cseries to CPU pin trace length<1250mil
d,12:4:6:4:12(1080 for 93ohm)



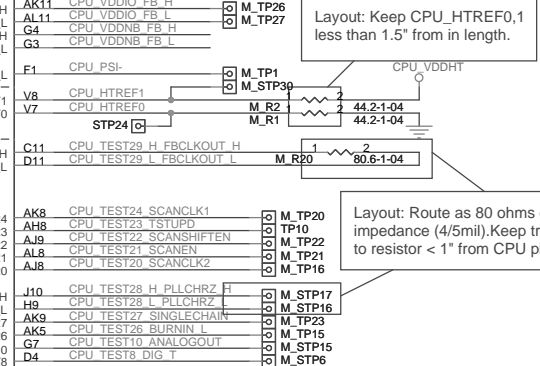
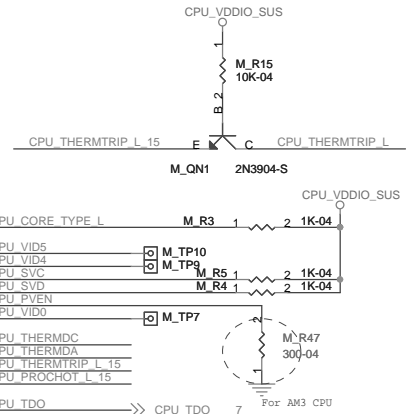
CPU

MISC.



INT. MISC.

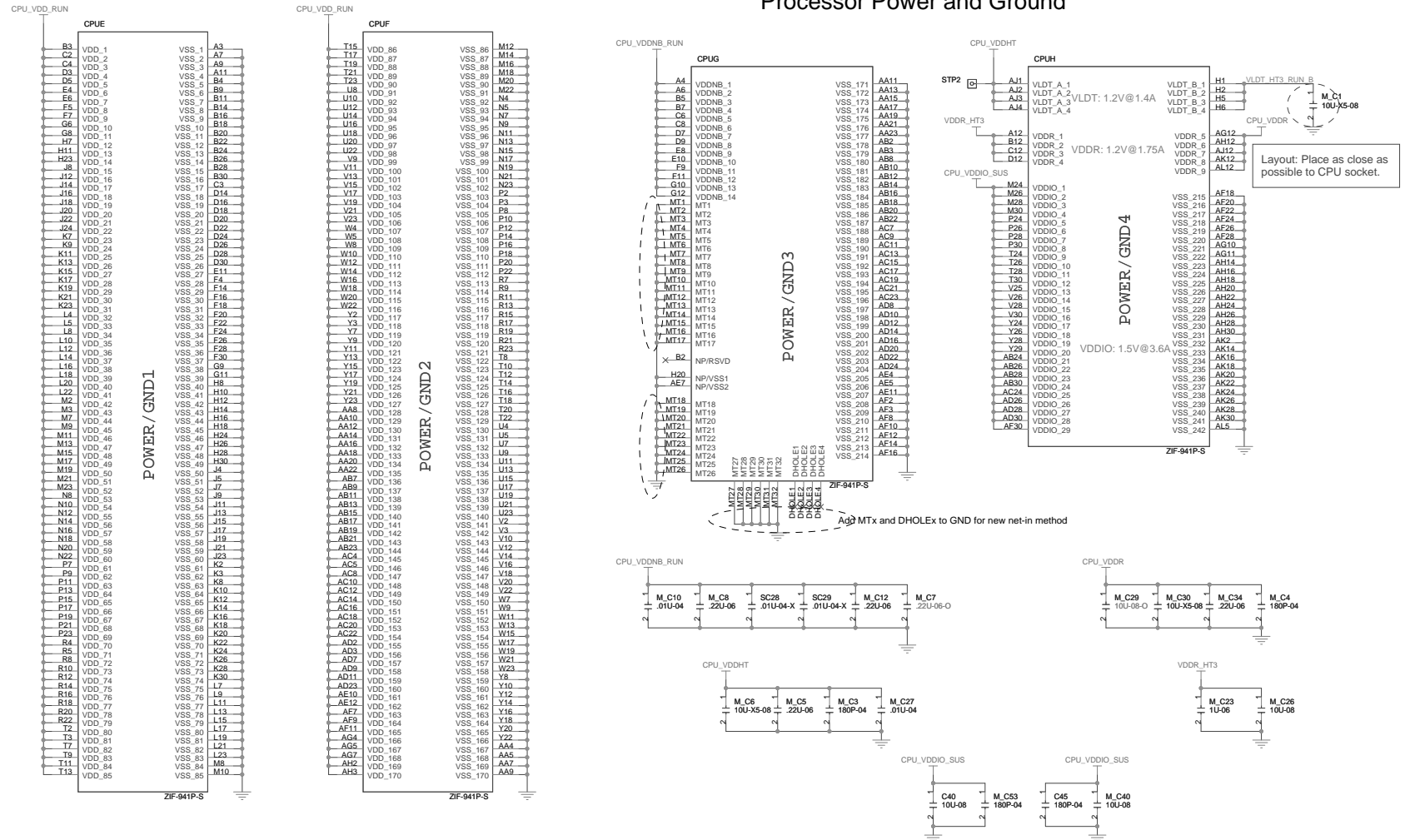
ZIF-941P-S



Elitegroup Computer Systems

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Timing diagram showing the relationship between VDDHT and VDDNB signals. The diagram shows VDDHT rising first, followed by VDDNB rising. The VDDHT signal is labeled with CPU_VDDHT and CPU_VDDHT. The VDDNB signal is labeled with CPU_VDDNB and CPU_VDDNB_RUN. The VDDHT signal is also labeled with CPU_VDDHT and CPU_VDDHT.



FOR EMC

VDDR_HT3

M_C24 22U-06

1 2

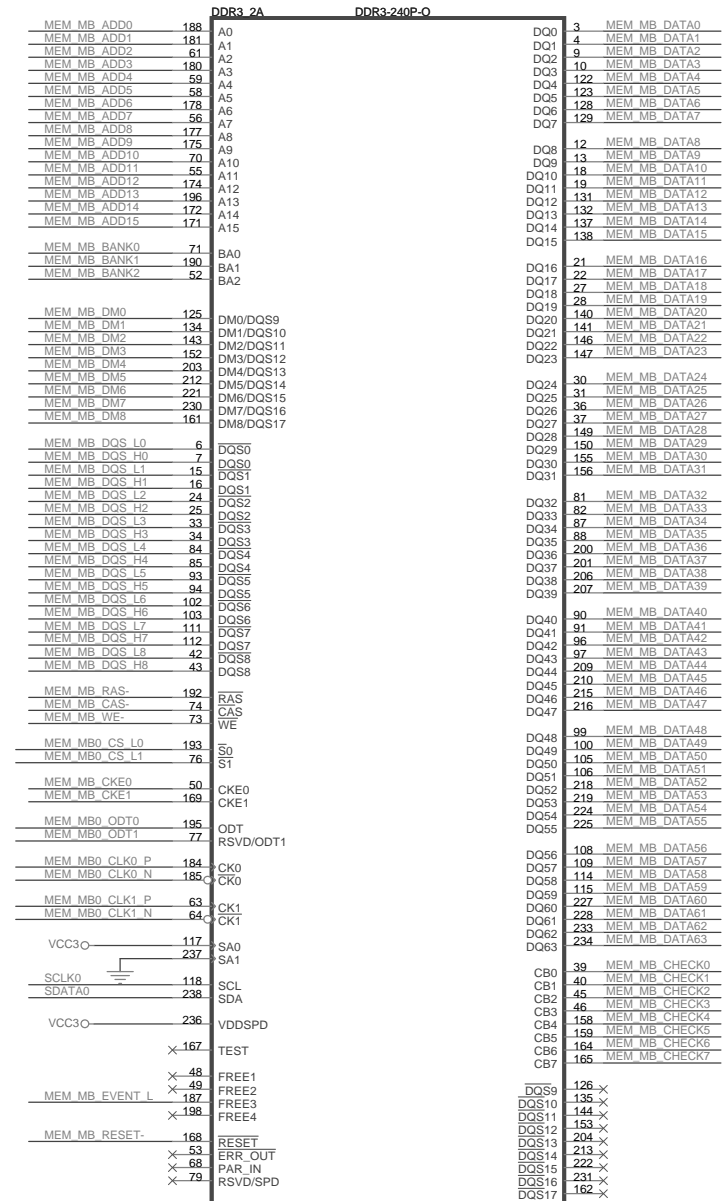
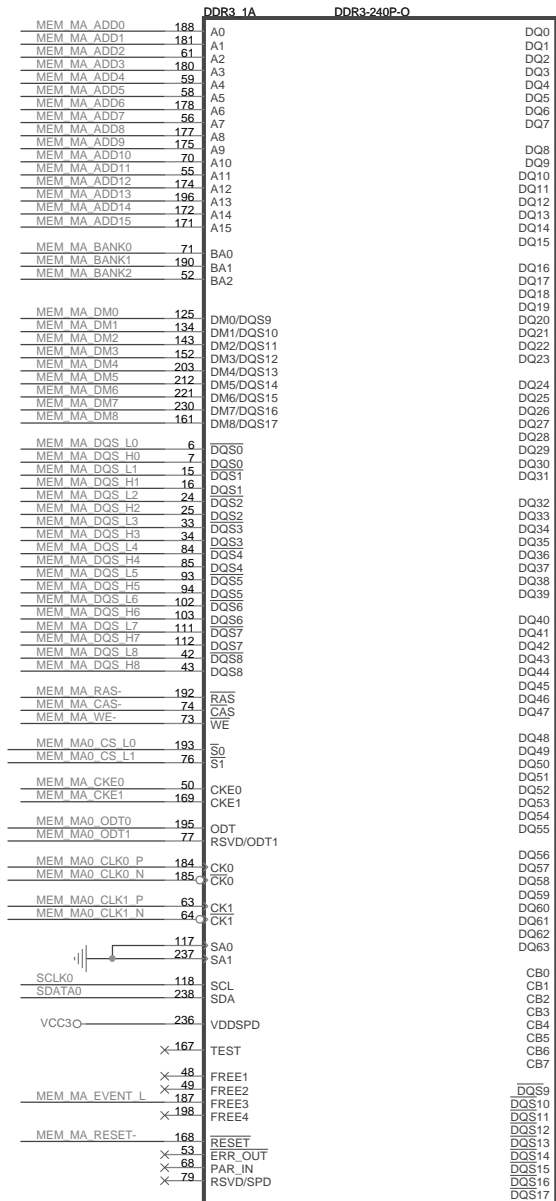
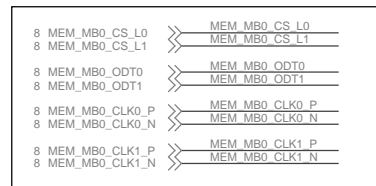
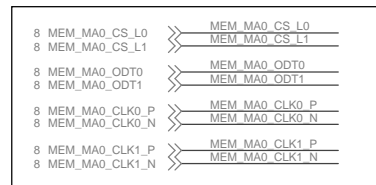
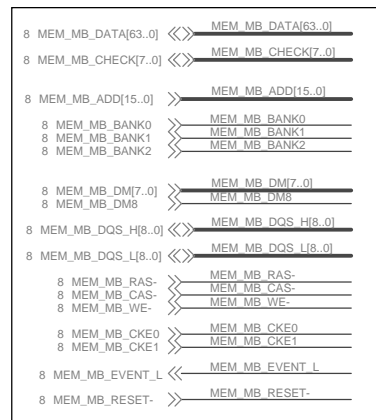
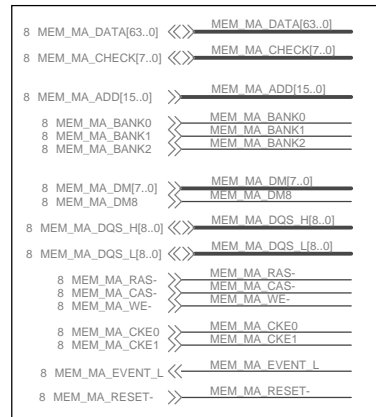
M_C25 22U-06

1 2

SC16 22U-06-X

CPU_VDDNB_RUN

M_C13 .1U-04



SMBus Addressing

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A1

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DDR3 DIMM CHANNEL

Size

Custom

Document Number

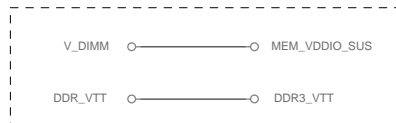
Rev

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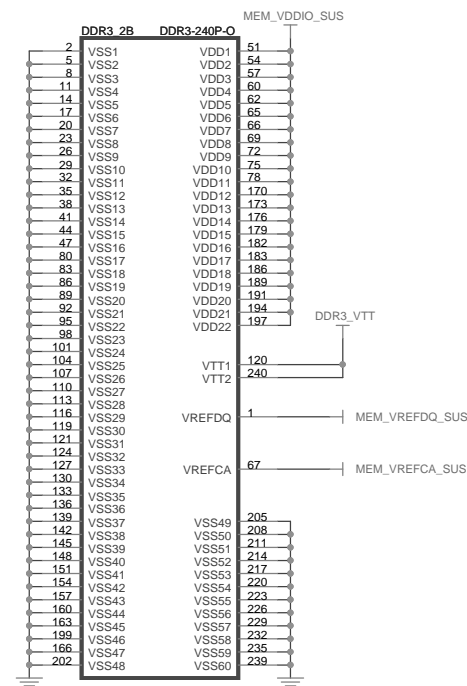
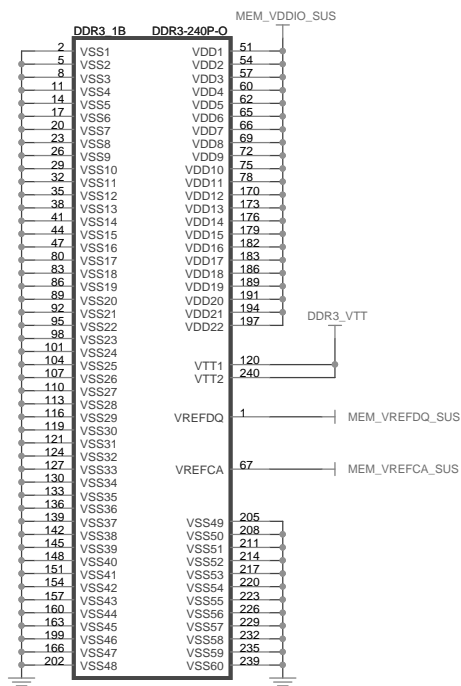
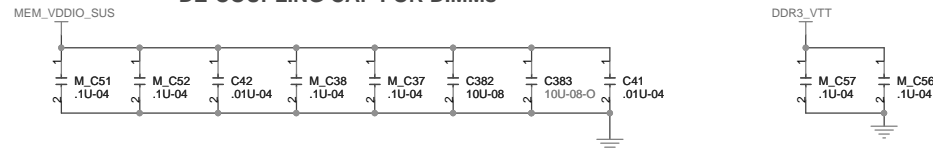
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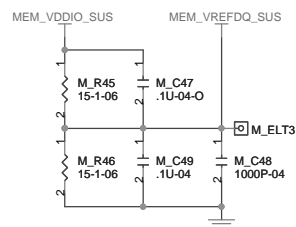
2.0



DE-COUPLING CAP FOR DIMMs

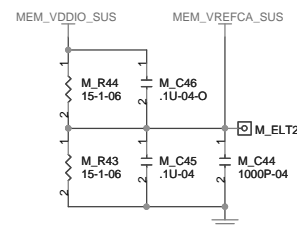


MEM_VREFDQ_SUS



Layout: Place within 500 mils of the DIMMB1 socket.
12mil(width):20mil(spacing)

MEM_VREFCA_SUS



Layout: Place within 500 mils of the DIMMB1 socket.
12mil(width):20mil(spacing)

HT LINK

7 HT_CLKIN_H[0..1]	>>	HT_CLKIN_P[0..1]
7 HT_CLKIN_L[0..1]	>>	HT_CLKIN_N[0..1]
7 HT_CLKOUT_H[0..1]	<<	HT_CLKOUT_P[0..1]
7 HT_CLKOUT_L[0..1]	<<	HT_CLKOUT_N[0..1]
7 HT_CTLIN_H[0..1]	>>	HT_CTLIN_P[0..1]
7 HT_CTLIN_L[0..1]	>>	HT_CTLIN_N[0..1]
7 HT_CTLOUT_H[0..1]	<<	HT_CTLOUT_P[0..1]
7 HT_CTLOUT_L[0..1]	<<	HT_CTLOUT_N[0..1]
7 HT_CADIN_H[0..15]	>>	HT_CADIN_P[0..15]
7 HT_CADIN_L[0..15]	>>	HT_CADIN_N[0..15]
7 HT_CADOUT_H[0..15]	<<	HT_CADOUT_P[0..15]
7 HT_CADOUT_L[0..15]	<<	HT_CADOUT_N[0..15]

NBA			
PART 1 OF 6			
HYPER TRANSPORT CPU I/F			
HT_CADOUT_P0	Y25	HT_RXCAD0P	D24
HT_CADOUT_N0	Y24	HT_RXCAD0N	D25
HT_CADOUT_P1	V22	HT_RXCAD1P	E24
HT_CADOUT_N1	V23	HT_RXCAD1N	E25
HT_CADOUT_P2	V24	HT_RXCAD2P	F24
HT_CADOUT_N2	V25	HT_RXCAD2N	F25
HT_CADOUT_P3	U24	HT_RXCAD3P	F23
HT_CADOUT_N3	U25	HT_RXCAD3N	F22
HT_CADOUT_P4	T25	HT_RXCAD4P	H23
HT_CADOUT_N4	T24	HT_RXCAD4N	H22
HT_CADOUT_P5	P22	HT_RXCAD5P	J25
HT_CADOUT_N5	P23	HT_RXCAD5N	J24
HT_CADOUT_P6	P25	HT_RXCAD6P	K24
HT_CADOUT_N6	P24	HT_RXCAD6N	K25
HT_CADOUT_P7	N24	HT_RXCAD7P	K23
HT_CADOUT_N7	N25	HT_RXCAD7N	K22
HT_CADOUT_P8	AC24	HT_RXCAD8P	F21
HT_CADOUT_N8	AC25	HT_RXCAD8N	G21
HT_CADOUT_P9	AB25	HT_RXCAD9P	G20
HT_CADOUT_N9	AB24	HT_RXCAD9N	H21
HT_CADOUT_P10	AA24	HT_RXCAD10P	J20
HT_CADOUT_N10	AA25	HT_RXCAD10N	J21
HT_CADOUT_P11	Y22	HT_RXCAD11P	J18
HT_CADOUT_N11	Y23	HT_RXCAD11N	K17
HT_CADOUT_P12	W21	HT_RXCAD12P	L19
HT_CADOUT_N12	W20	HT_RXCAD12N	J19
HT_CADOUT_P13	V21	HT_RXCAD13P	M19
HT_CADOUT_N13	V20	HT_RXCAD13N	L18
HT_CADOUT_P14	U20	HT_RXCAD14P	M21
HT_CADOUT_N14	U21	HT_RXCAD14N	P21
HT_CADOUT_P15	U19	HT_RXCAD15P	P18
HT_CADOUT_N15	U18	HT_RXCAD15N	M18
HT_CLKOUT_P0	T22	HT_RXCLK0P	H24
HT_CLKOUT_N0	T23	HT_RXCLK0N	H25
HT_CLKOUT_P1	AB23	HT_RXCLK1P	L21
HT_CLKOUT_N1	AA22	HT_RXCLK1N	L20
HT_CTLOUT_P0	M22	HT_RXCTL0P	M24
HT_CTLOUT_N0	M23	HT_RXCTL0N	M25
HT_CTLOUT_P1	R21	HT_RXCTL1P	P19
HT_CTLOUT_N1	R20	HT_RXCTL1N	R18
HT_RXCALP	C23	HT_TXCALP	B24
HT_RXCALN	A24	HT_TXCALN	B25

EP32
301-1-04

1 HT_RXCALP
HT_RXCALN

C23
A24

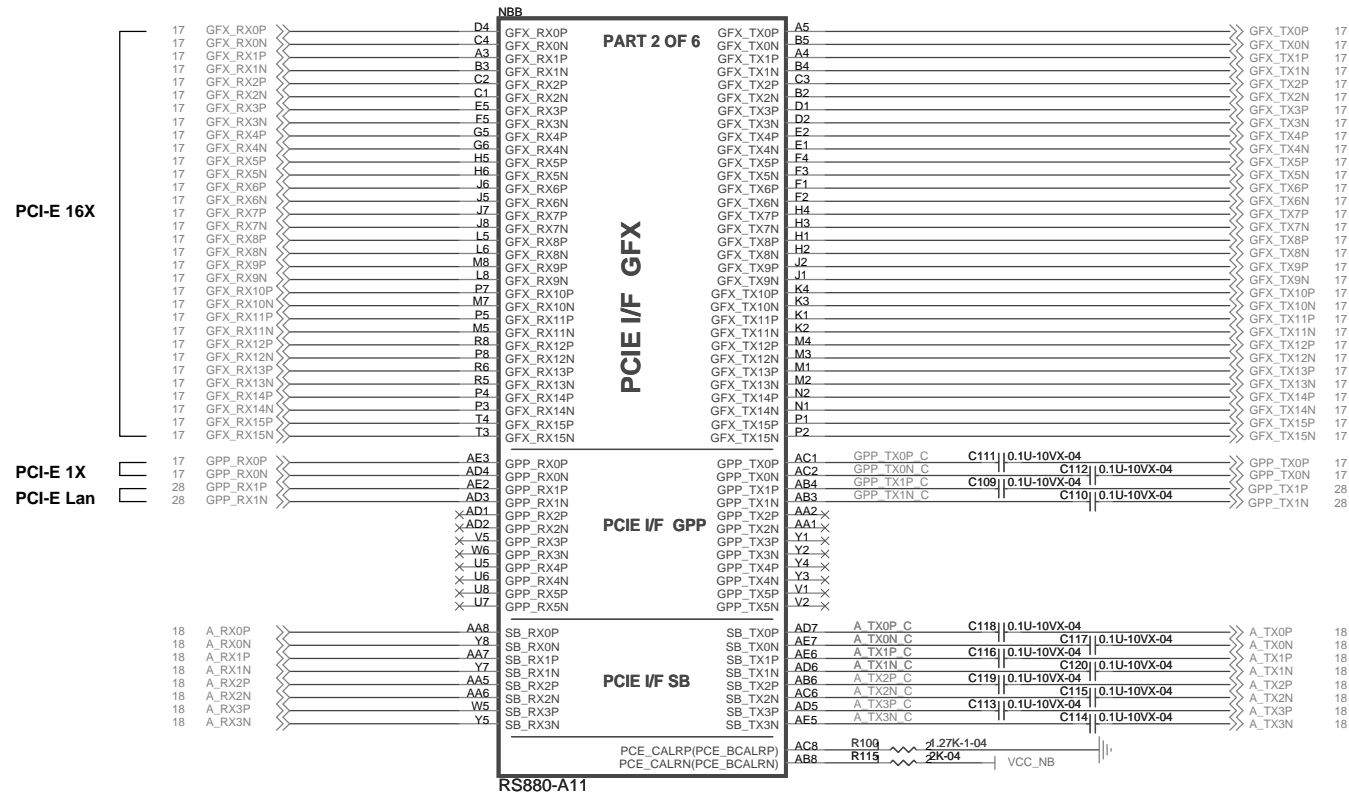
RS880-A11

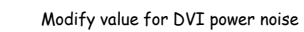
HT_TXCALP
HT_TXCALN

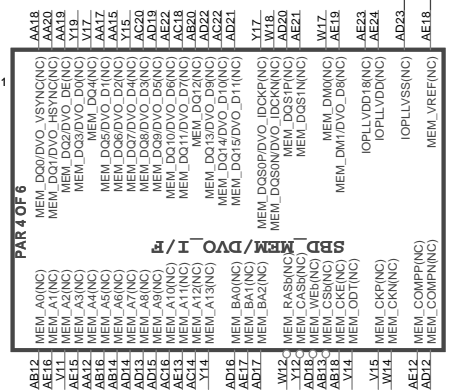
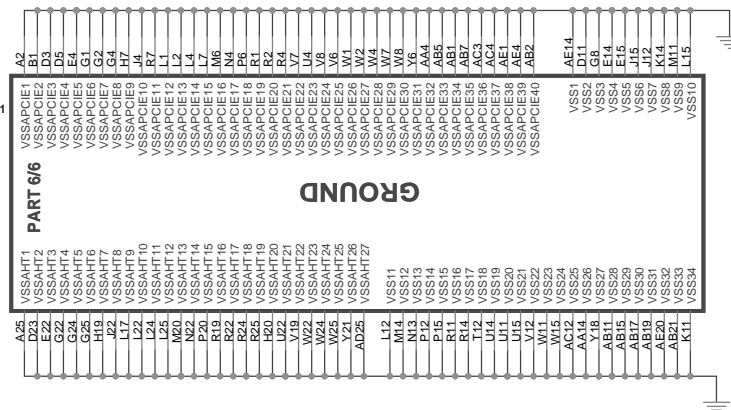
R76 1 301-1-04
HT_TXCALN

TX signals return path CAP , Placed near the North Bridge

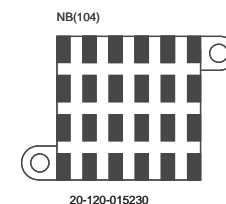






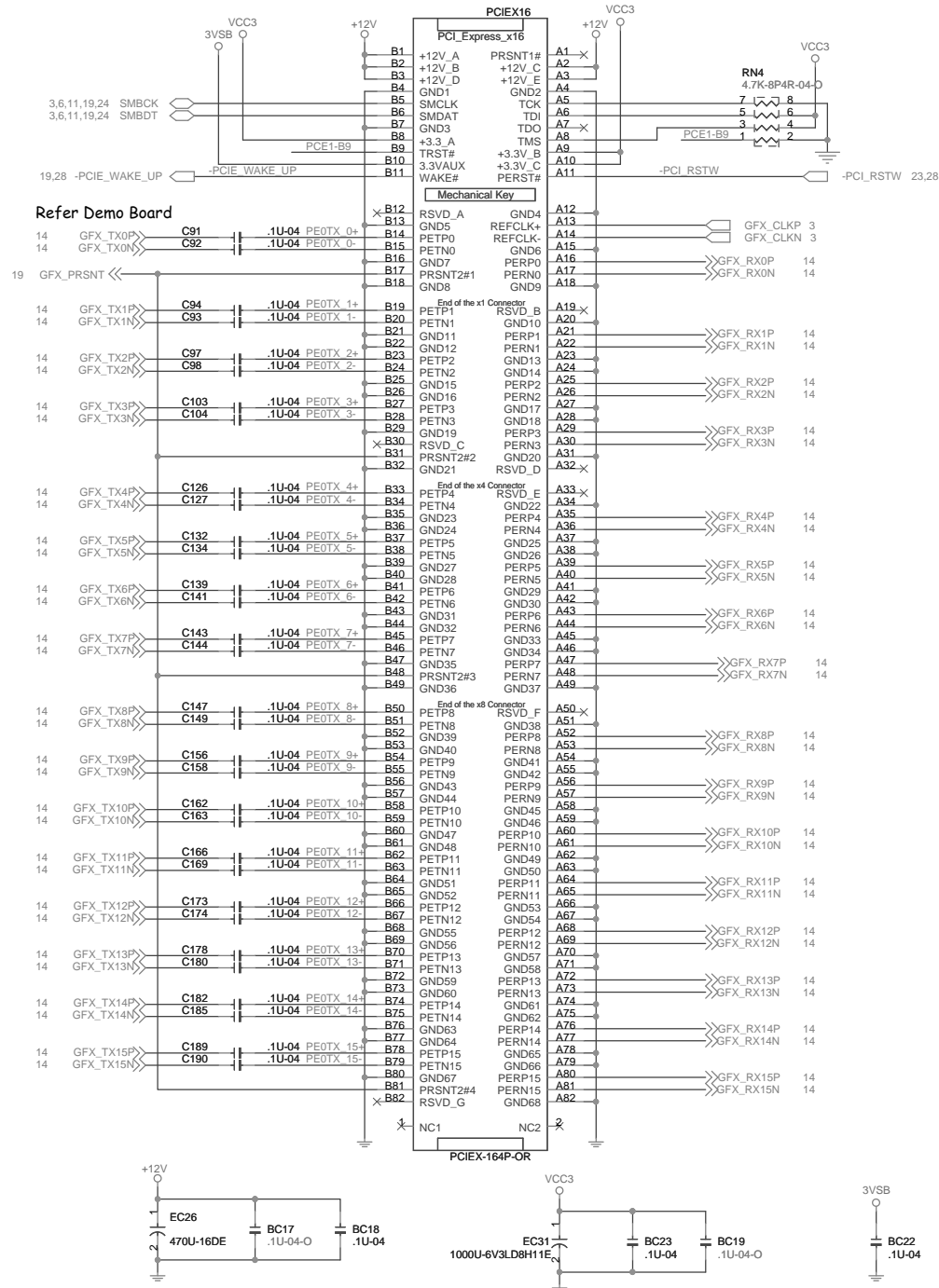


PIN NAME		RS880	VCC_NB: 1.1V	
VCC1.8V: 1.8V			VDDHT	0.6A
VDDA18PCIE	0.7A	VDDHTRX	0.7A	
VDD18	0.01A	VDDPCIE	2.5A	
VDD18_MEM	0.025A	VDDC	13A	
PLLVD18	0.02A	PLLVD	0.065A	
VDDA18HTPLL	0.02A	Total	16.865A	
VDDA18PCIEPLL	0.12A	VCC3		
VDDLTP18	0.015A	VDD33	0.06A	
VDDL18	0.3A	AVDD	0.11A	
AVDDI	0.02A	Total	0.17A	
AVDDQ	0.004A	VDDHT: 1.2V		
Total	1.234A	VDDHTTX	0.4A	



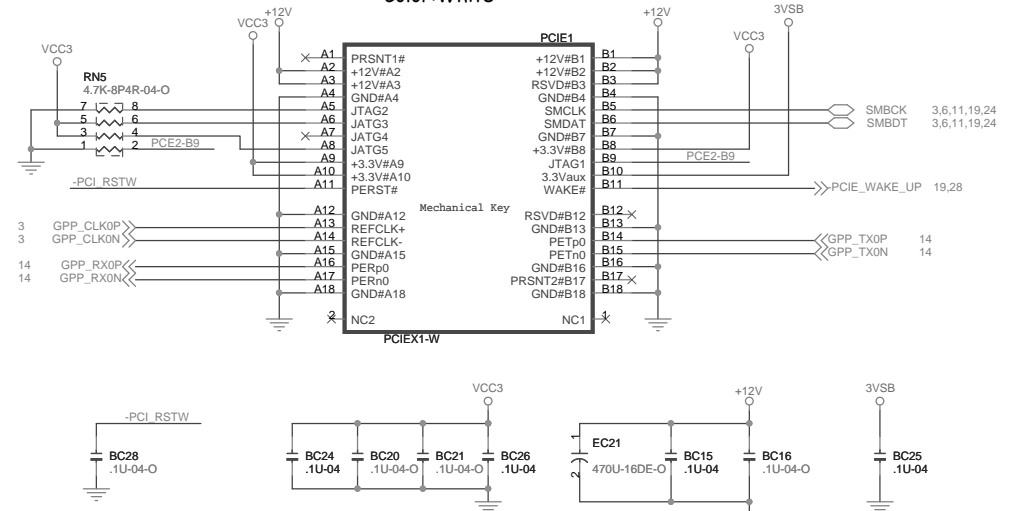
PCI_EXPRESS_x16

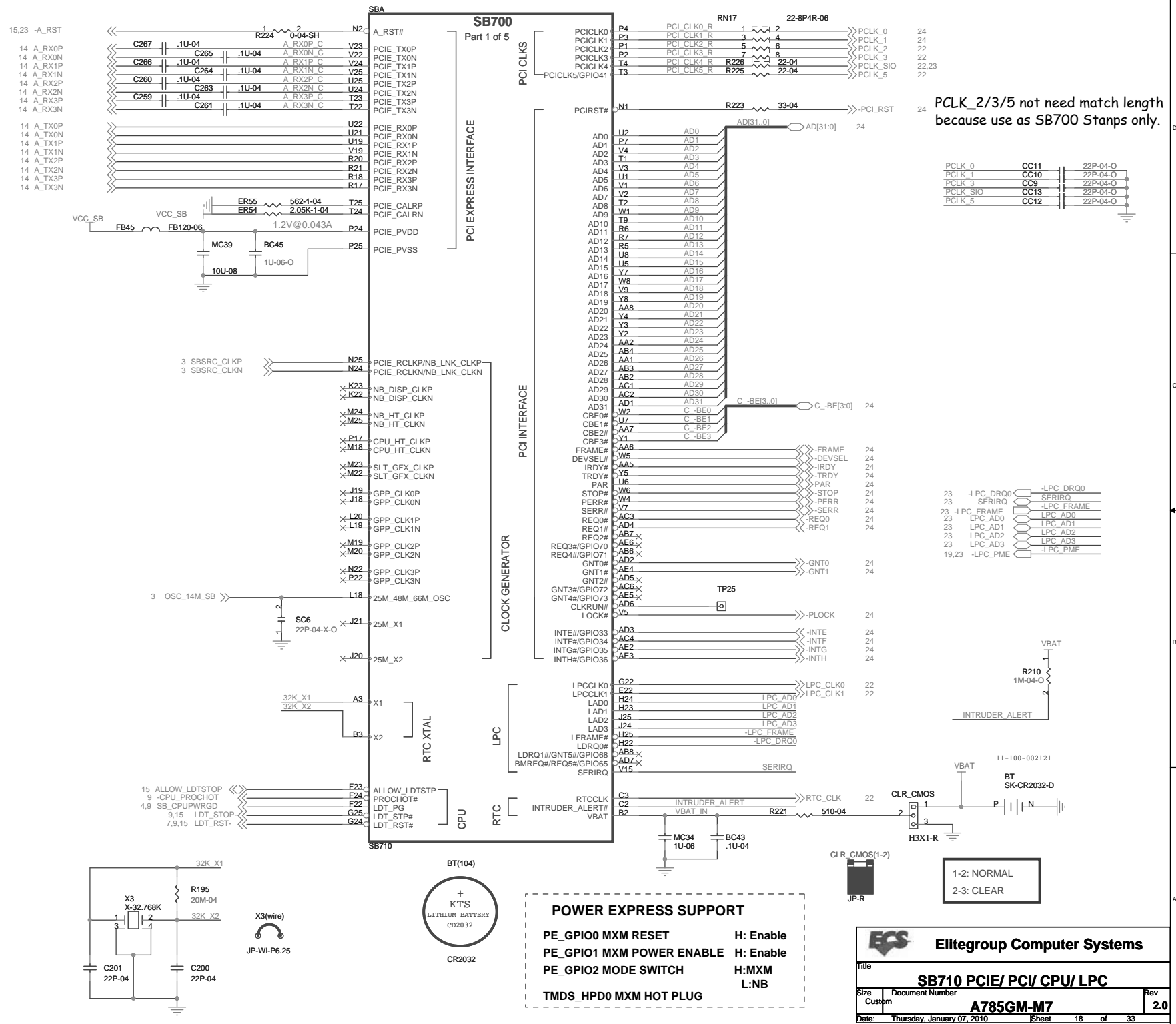
Color:Orange +12V:5.5Amp

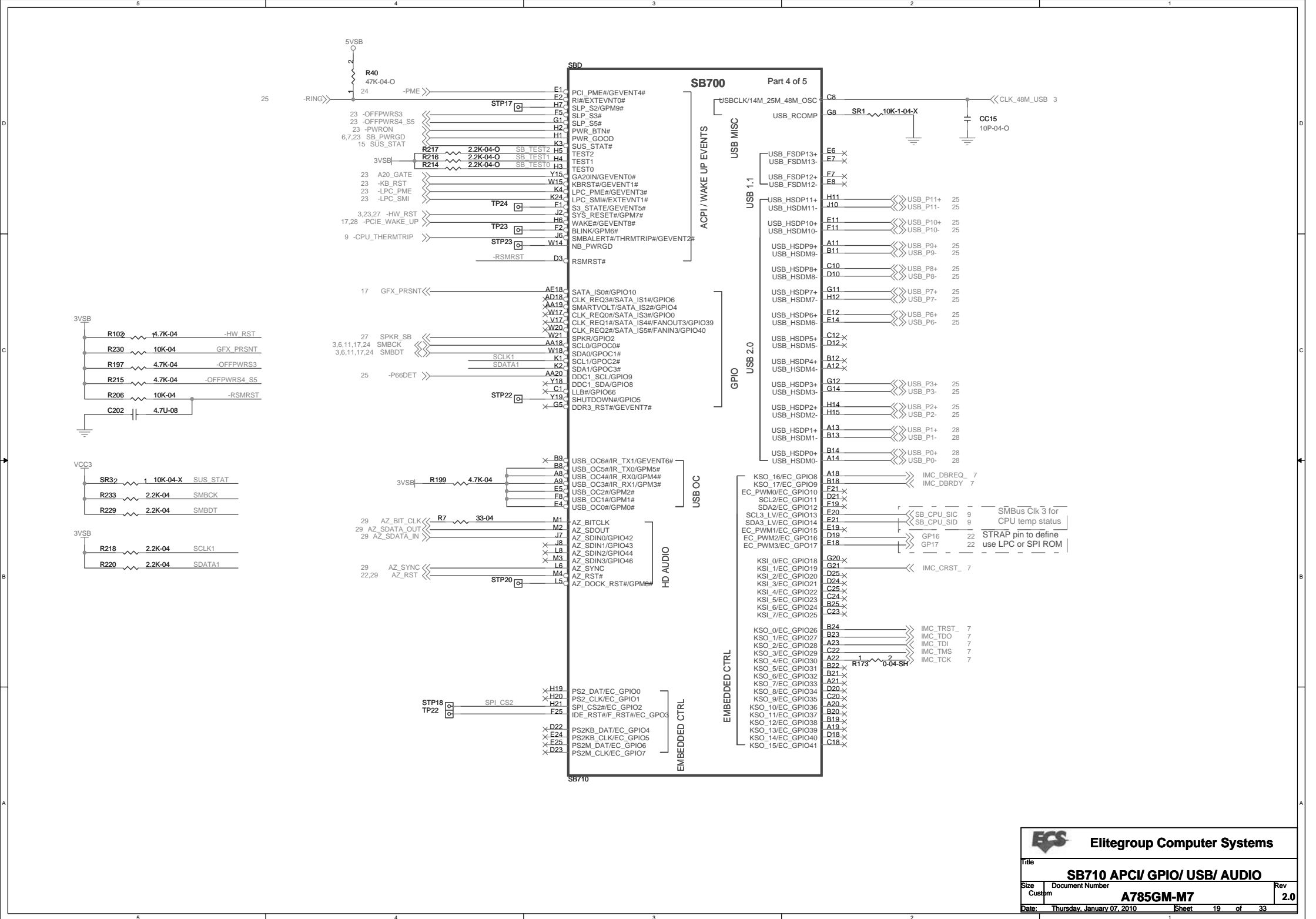


PCI_EXPRESS_x1

Color:White





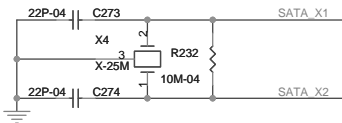


PLACE SATA AC COUPLING
CAPS CLOSE TO SB700

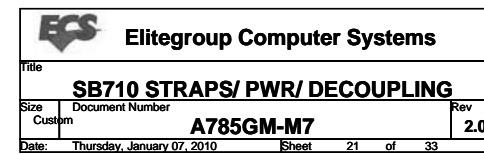
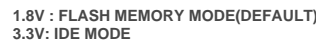
SATA TX0+	C320	.01U-04	AD9	SATA_TX0+
SATA TX0-	C326	.01U-04	AE9	SATA_TX0-
SATA RX0-	C333	.01U-04	AB10	SATA_RX0-
SATA RX0+	C339	.01U-04	AC10	SATA_RX0+
SATA TX1+	C319	.01U-04	AE10	SATA_TX1+
SATA TX1-	C325	.01U-04	AD10	SATA_TX1-
SATA RX1-	C338	.01U-04	AD11	SATA_RX1-
SATA RX1+	C343	.01U-04	AE11	SATA_RX1+
SATA TX2+	C312	.01U-04	AB12	SATA_TX2+
SATA TX2-	C318	.01U-04	AC12	SATA_TX2-
SATA RX2-	C330	.01U-04	AE12	SATA_RX2-
SATA RX2+	C331	.01U-04	AD12	SATA_RX2+
SATA TX3+	C321	.01U-04	AD13	SATA_TX3+
SATA TX3-	C327	.01U-04	AE13	SATA_TX3-
SATA RX3-	C334	.01U-04	AB14	SATA_RX3-
SATA RX3+	C340	.01U-04	AC14	SATA_RX3+
SATA TX4+	C322	.01U-04	AE14	SATA_TX4+
SATA TX4-	C328	.01U-04	AD14	SATA_TX4-
SATA RX4-	C335	.01U-04	AD15	SATA_RX4-
SATA RX4+	C341	.01U-04	AE15	SATA_RX4+
SATA TX5+	C323	.01U-04	AB16	SATA_TX5+
SATA TX5-	C329	.01U-04	AC16	SATA_TX5-
SATA RX5-	C336	.01U-04	AD16	SATA_RX5-
SATA RX5+	C342	.01U-04	AE16	SATA_RX5+

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB700

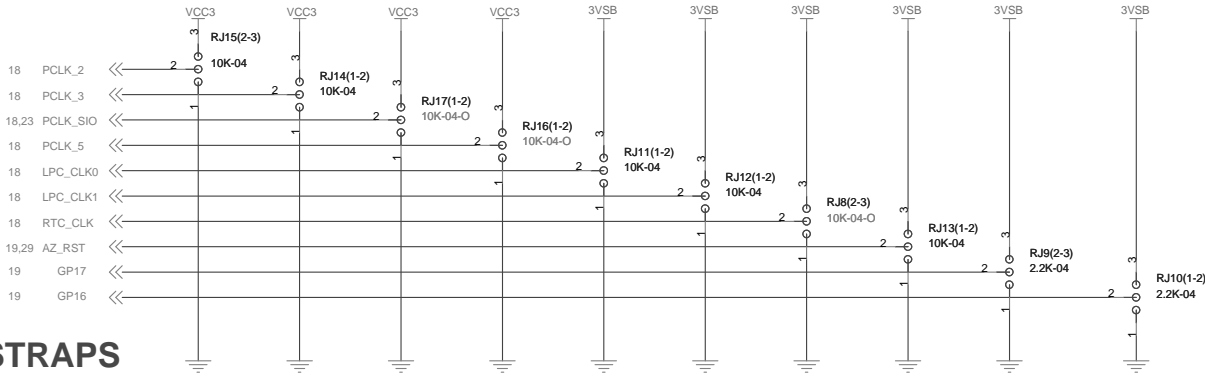
NOTE:
SR2 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK



PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE



NOTE: SB710 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

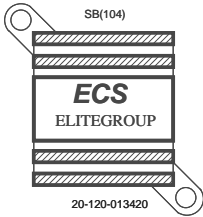


REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
	Watchdog ENABLED DEFAULT	USE DEBUG STRAPS	RESERVED	RESERVED	IMC Enable	CLKGEN ENABLED	INTERNAL RTC DEFAULT	PCI ROM BOOT Enable	ROM TYPE: H, H = Reserved H, L = SPI ROM	DEFAULT
PULL LOW	Watchdog DISABLED	IGNORE DEBUG STRAPS DEFAULT			IMC Disable DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	PCI ROM BOOT Disable DEFAULT	L, H = LPC ROM L, L = FWH ROM	

A12

A12



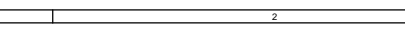
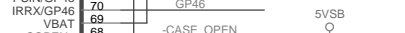
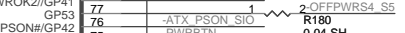
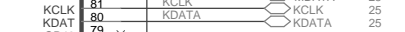
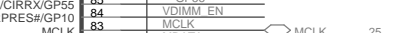
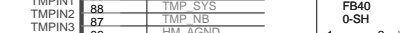
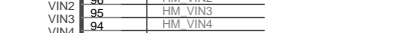
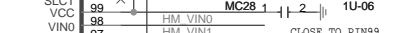
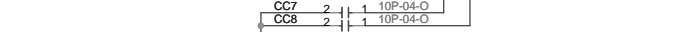
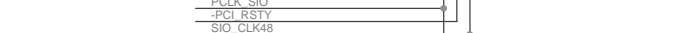
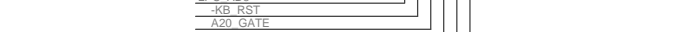
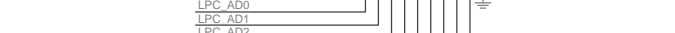
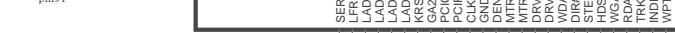
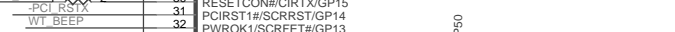
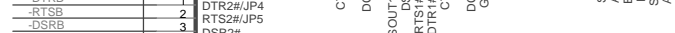
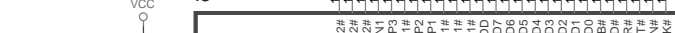
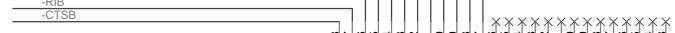
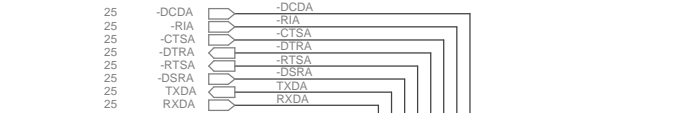
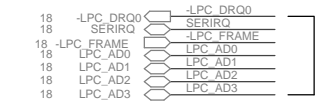
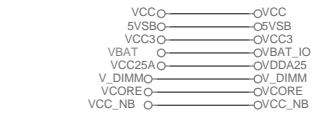
SB710 POWER TABLE

PIN NAME	SB710	PIN NAME	SB710
VCC_SB: 1.2V		VCC3	
PCIE_PVDD	0.043A	XTLVDD_SATA	0.006A
PLLVD_SATA	0.093A	VDDQ	0.131A
PCIE_VDDR	0.6A	VDD33_18	0.071A
AVDD_SATA	0.567A	AVDDCK_3.3V	0.047A
VDD	0.51A	Total	0.255A
CKVDD_1.2V		3VSB	
AVDDCK_1.2V	0.062A	AVDDTX/RX	0.658A
Total	1.875A	AVDDC	0.017A
1.2VSB		S5_3.3V	0.032A
S5_1.2V	0.113A	Total	0.707A
USB_PHY_1.2V		5VSB	
Total	0.31A	V5_VREF	0.001A

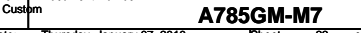
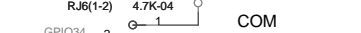
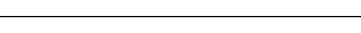
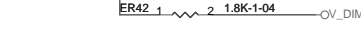
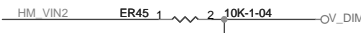
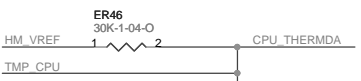
Elitegroup Computer Systems

SB710 Straps			
Size Custom	Document Number A785GM-M7		Rev 2.0
Date:	Thursday, January 07, 2010		Sheet 22 of 33

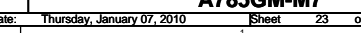
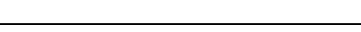
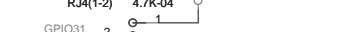
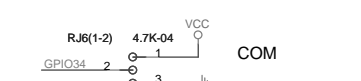
External Connection



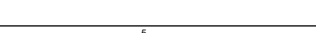
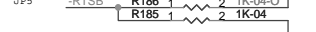
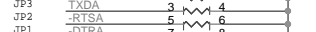
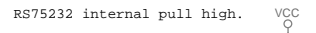
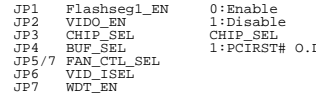
Thermal Monitor



BIOS SELECTION

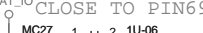
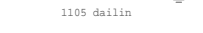
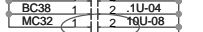
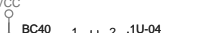
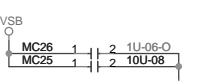


HW STRAPPING

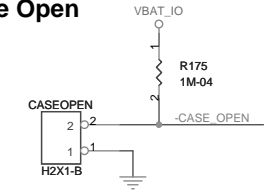


BYPASS CAP

CLOSE TO PIN67



Case Open

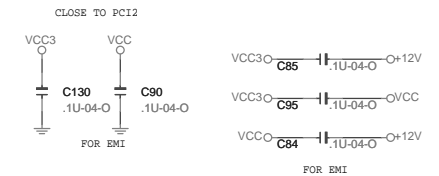
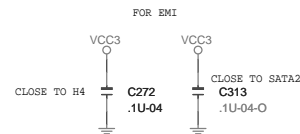
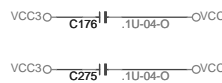
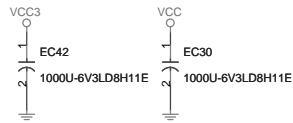
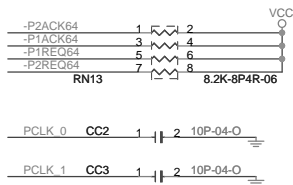
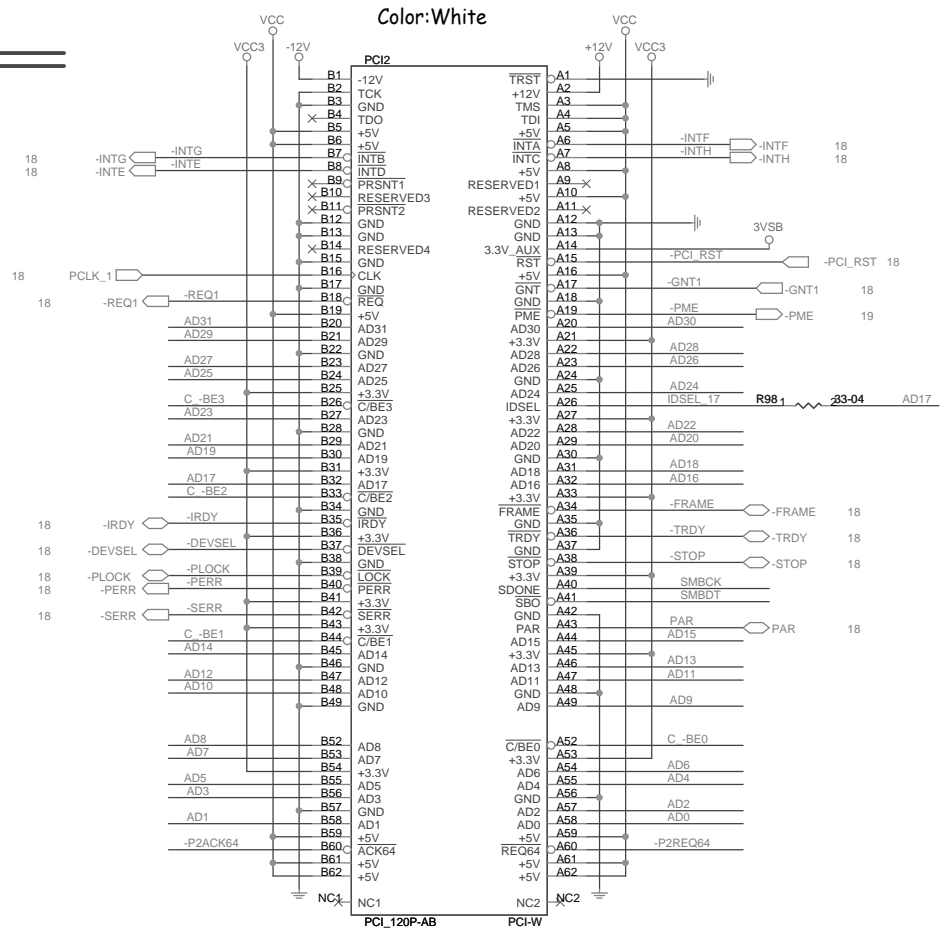
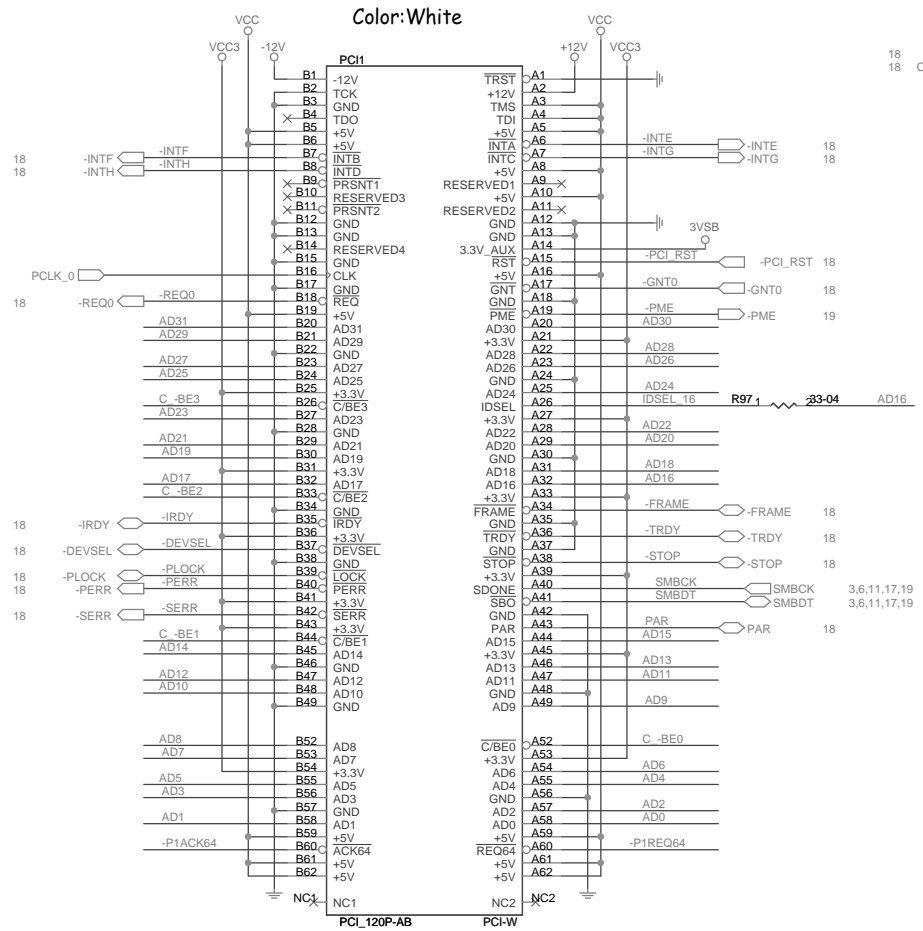


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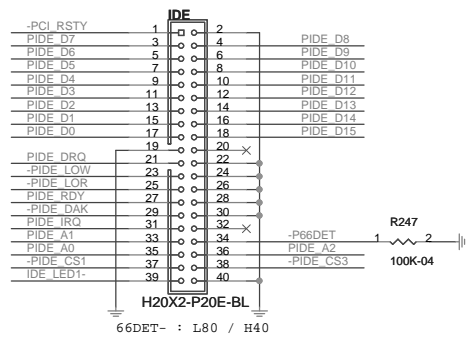
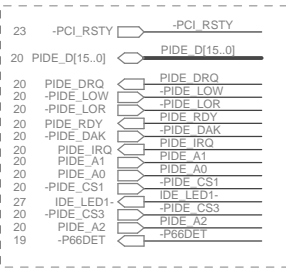
Title **LPC SIO - ITE726F/IX,ROM**

Size Document Number **A785GM-M7** Rev **2.0**

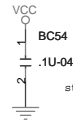
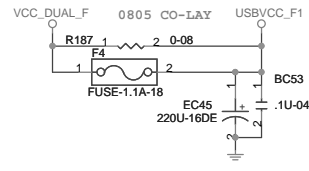
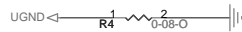
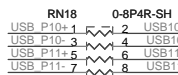
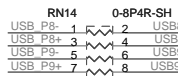
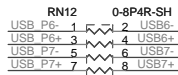
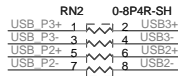
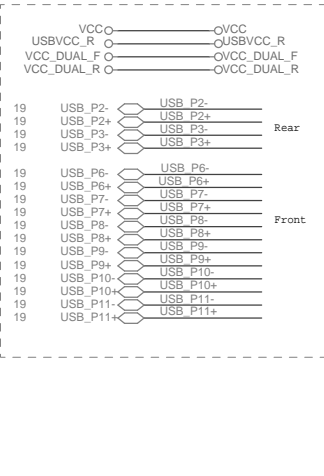
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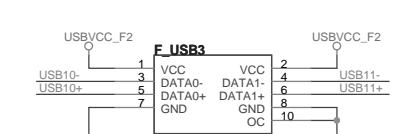
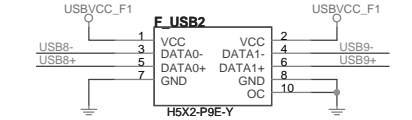
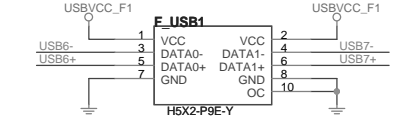
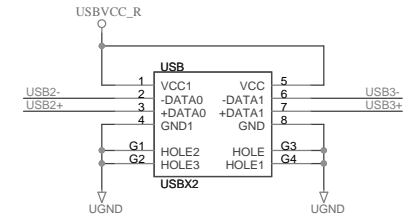
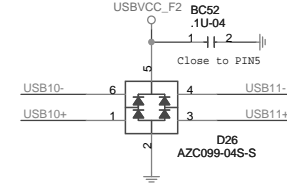
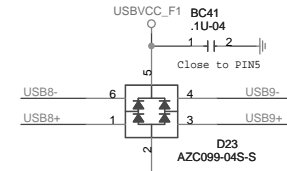
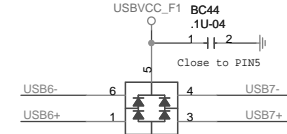
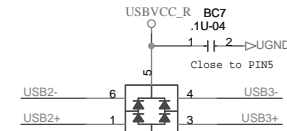
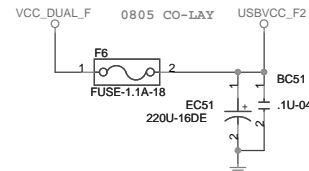
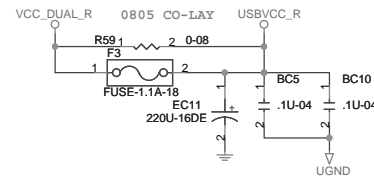
External Connection



External Connection

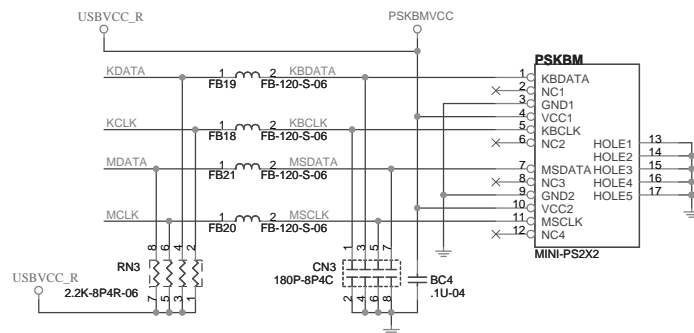
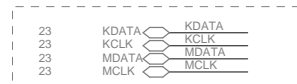


stitching Cap for USB



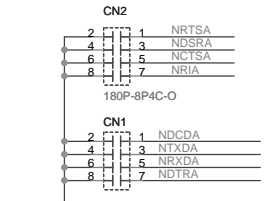
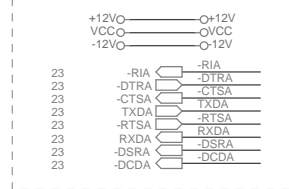
PSKBM

External Connection

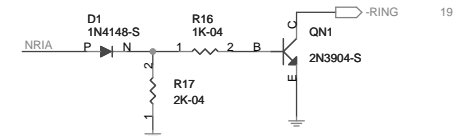
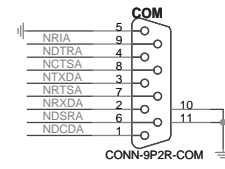
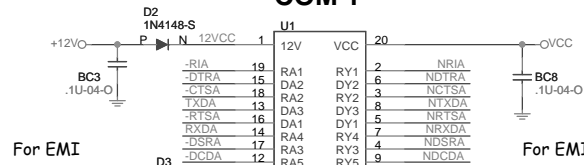


COM Ports

External Connection

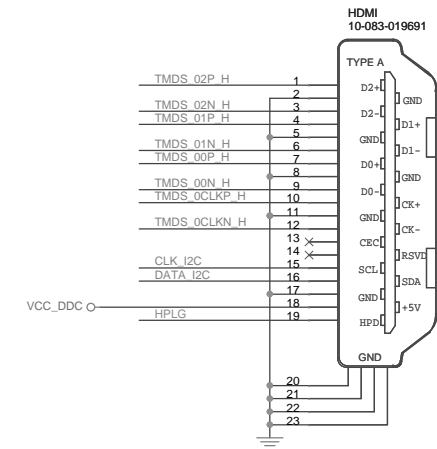
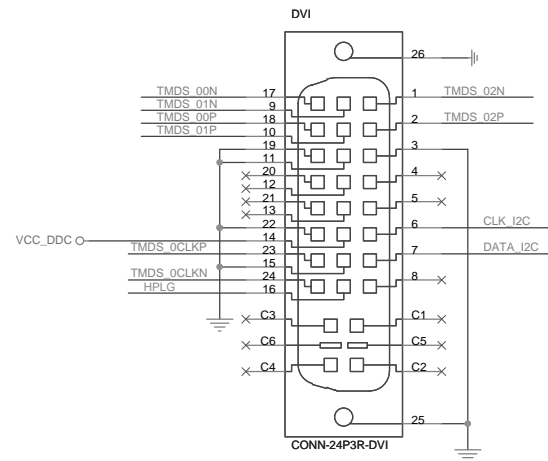
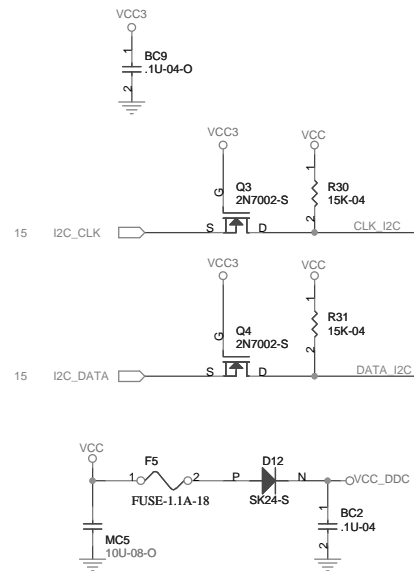
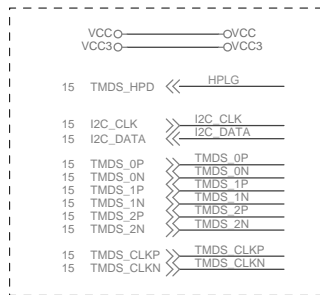


COM 1



Title IDE,USB, PSKBM,COM		
Size	Document Number	Rev
Custon	A785GM-M7	2.0
Date	Thursday, January 07, 2010	Sheet 25 of 33

External Connection



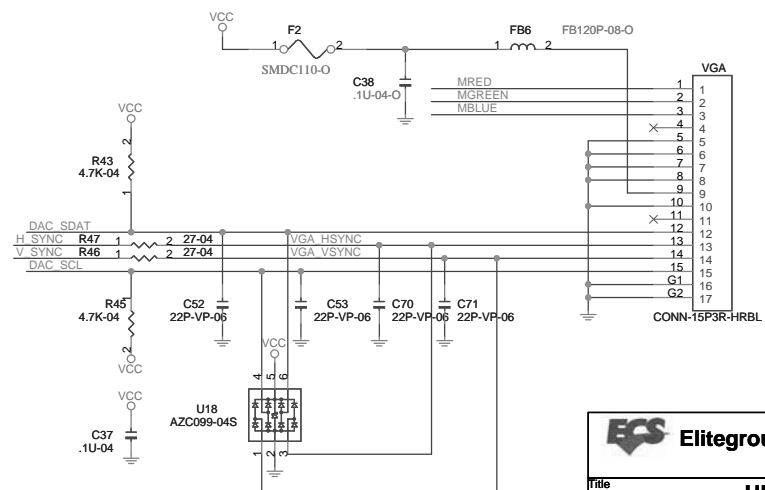
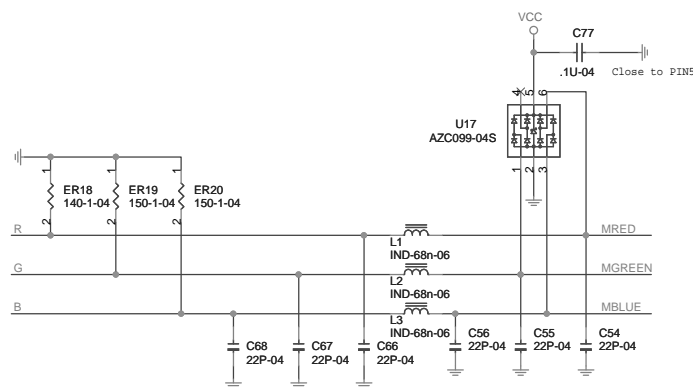
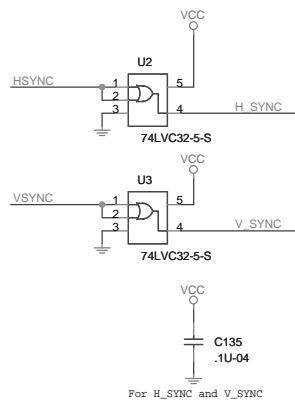
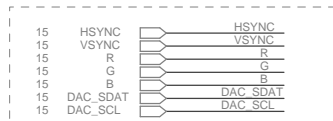
		RN6	CMK-90-1206
TMDS 2N	1	1	2 TMDS 02N
TMDS 2P	3	3	4 TMDS 02P
TMDS 1N	5	5	6 TMDS 01N
TMDS 1P	7	7	8 TMDS 01P

		SRN1	CMK-90-1206-O
TMDS 1P	1	1	2 TMDS 01P H
TMDS 1N	3	3	4 TMDS 01N H
TMDS 2P	5	5	6 TMDS 02P H
TMDS 2N	7	7	8 TMDS 02N H

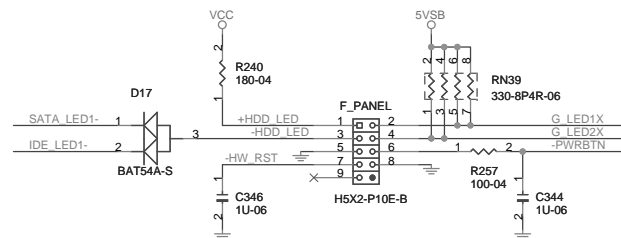
		RN7		CMK-90-1206	
TMDS_0N	1	1	2	2	TMDS_00N
TMDS_0P	3	3	4	4	TMDS_00P
TMDS_CLKP	5	5	6	6	TMDS_0CLKP
TMDS_CLKN	7	7	8	8	TMDS_0CLKN

SRN2		CMK-90-1206-O	
TMDS CLKN	1	2	TMDS_0CLKN H
TMDS CLKP	3	4	TMDS_0CLKP H
TMDS_0P	5	6	TMDS_00P H
TMDS_0N	7	8	TMDS_00N H

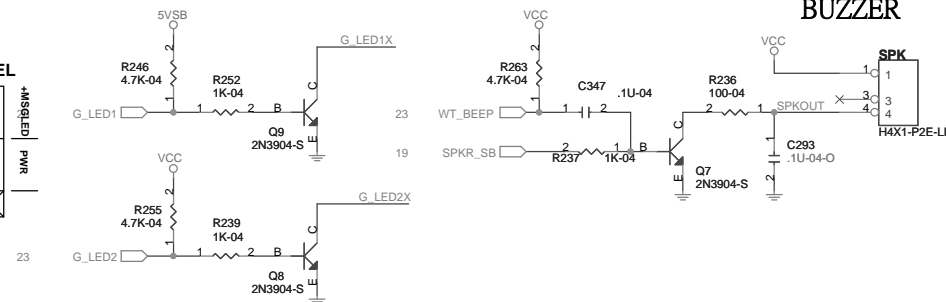
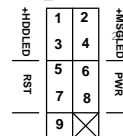
External Connection



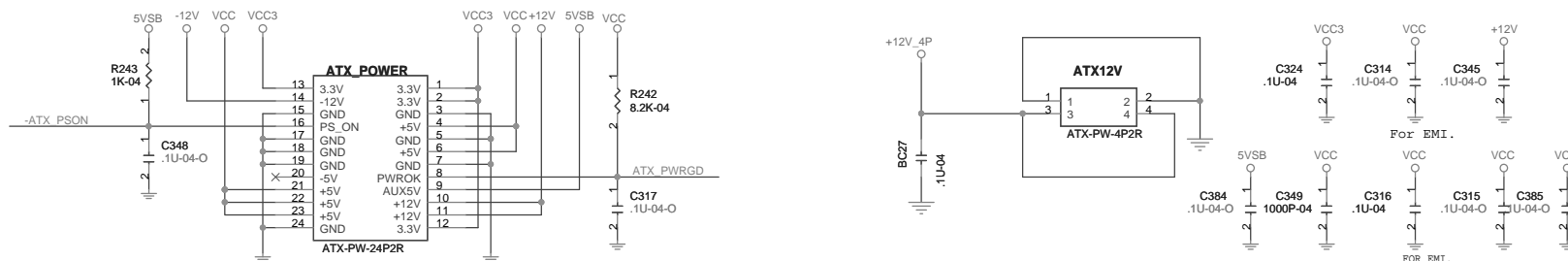
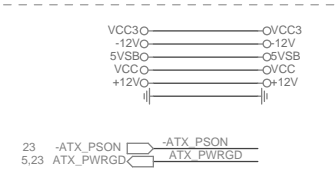
External Connection



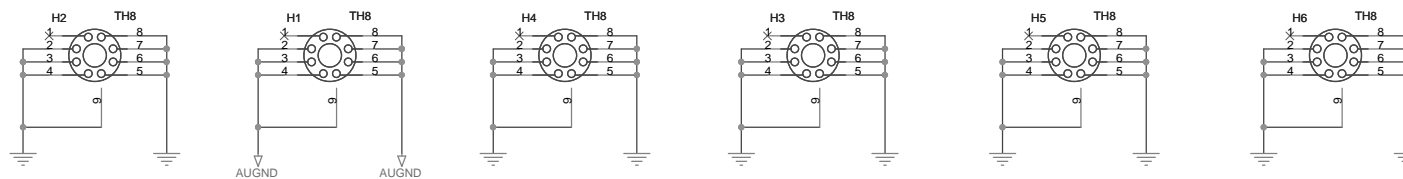
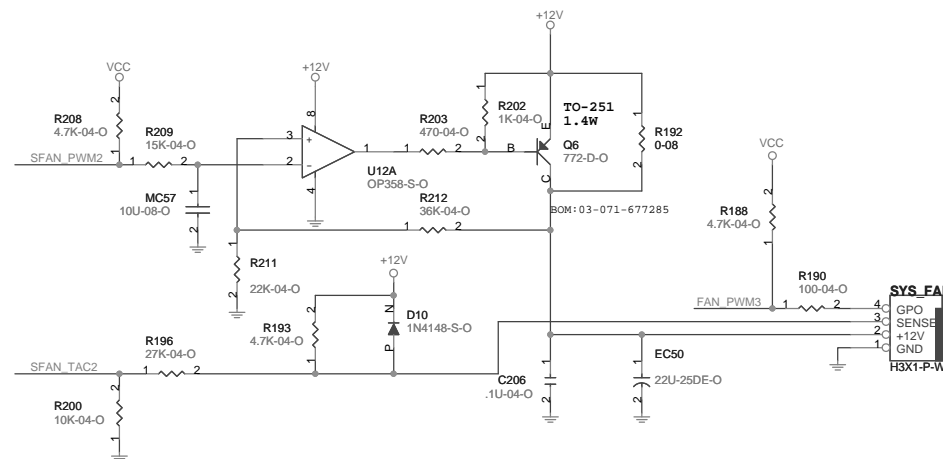
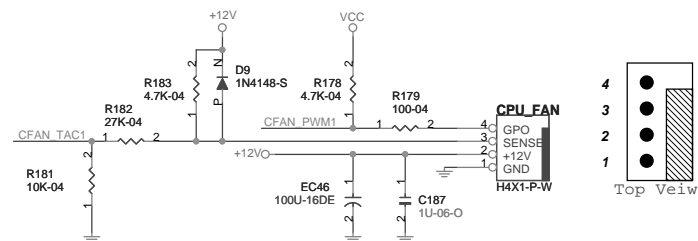
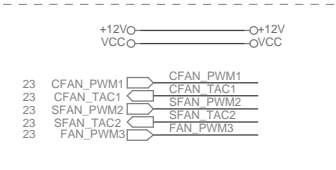
F_PANEL



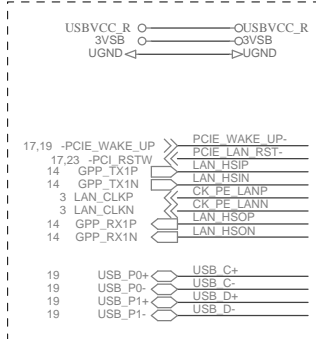
External Connection



External Connection



External Connection

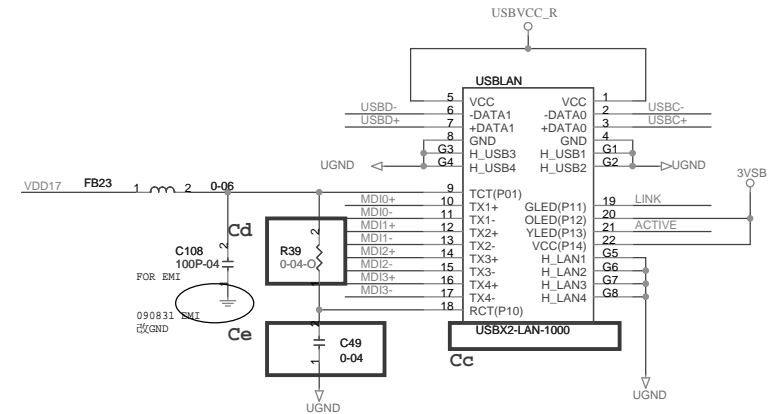
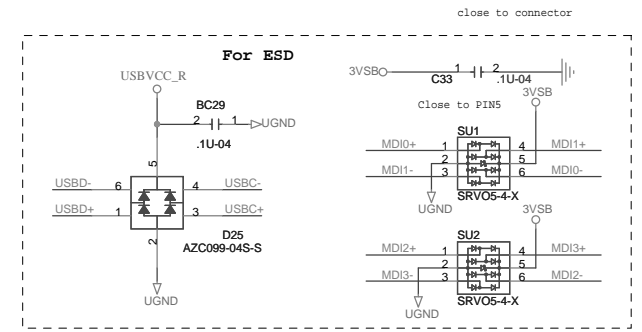
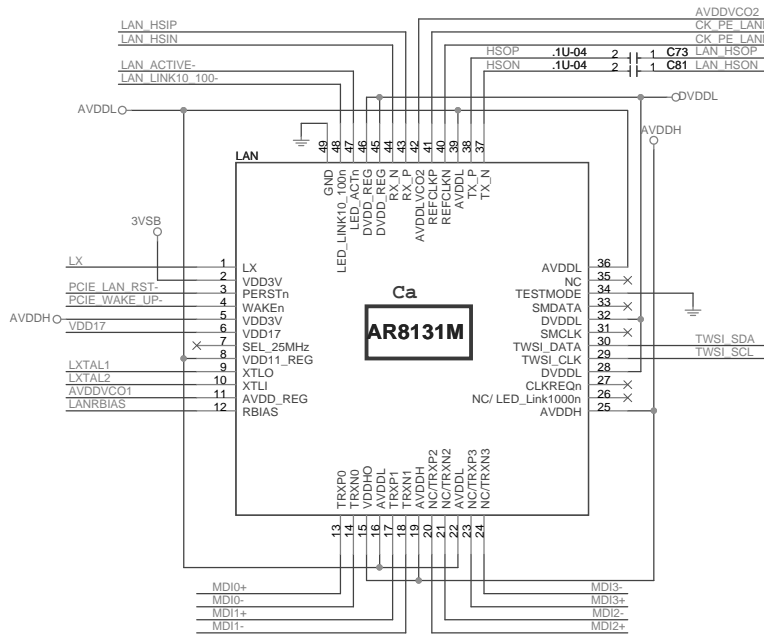


新手提醒:

LAN_HSOP/N請接到SB的PCIE RX端

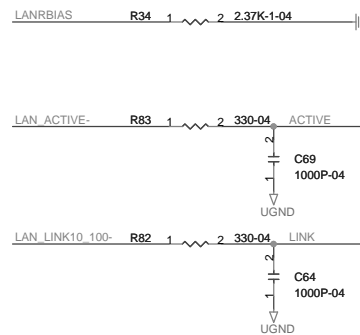
LAN_HSIP/N請接到SB的PCIE TX端

LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap



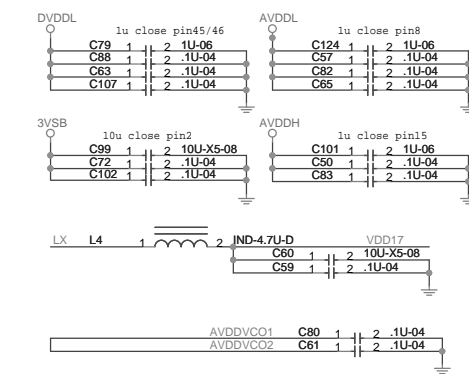
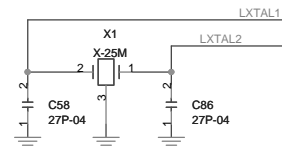
BOM Difference

	AR8132M AR8132	AR8131M AR8131	LAN with EEPROM on chip AR8132	LAN without EEPROM on chip (need external) AR8131
Ca	AR8132M	AR8131M	AR8132	AR8131
Cb	X	V	X	V
Cc	USBX2-LAN-100	USBX2-LAN-1000	USBX2-LAN-100	USBX2-LAN-1000
Cd	V	X	V	X
Ce	.01U-04	0-04	.01U-04	0-04
Cg	X	X	V	V
Ch	0-04	0-04	4.7K-04	4.7K-04
Ci	V	V	X	X

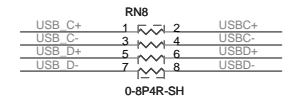


Power Difference

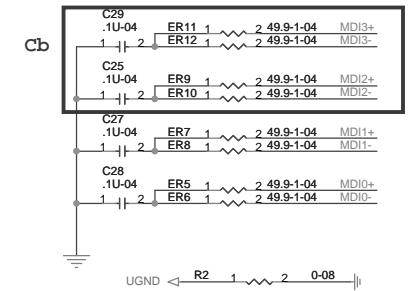
3VSB	3.3V 3VSB供應
AVDDL	1.1/1.15V pin8供應
DVDDL	1.1V pin45,46供應
AVDDH	2.5V pin15供應
VDD17	1.7V pin1供應
AVDDVCO2	1.2V pin12供應



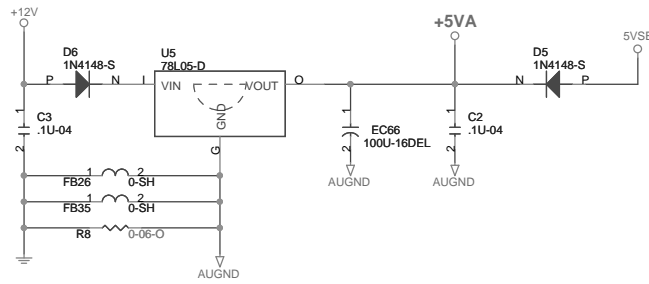
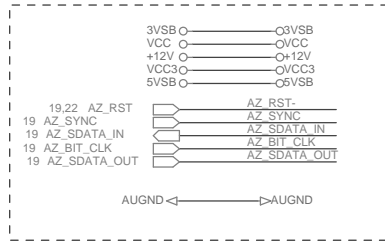
Link 10/100/1000: Active: Green on Yellow blinking



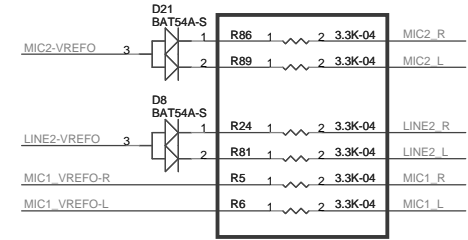
All terminator close to LAN chip.



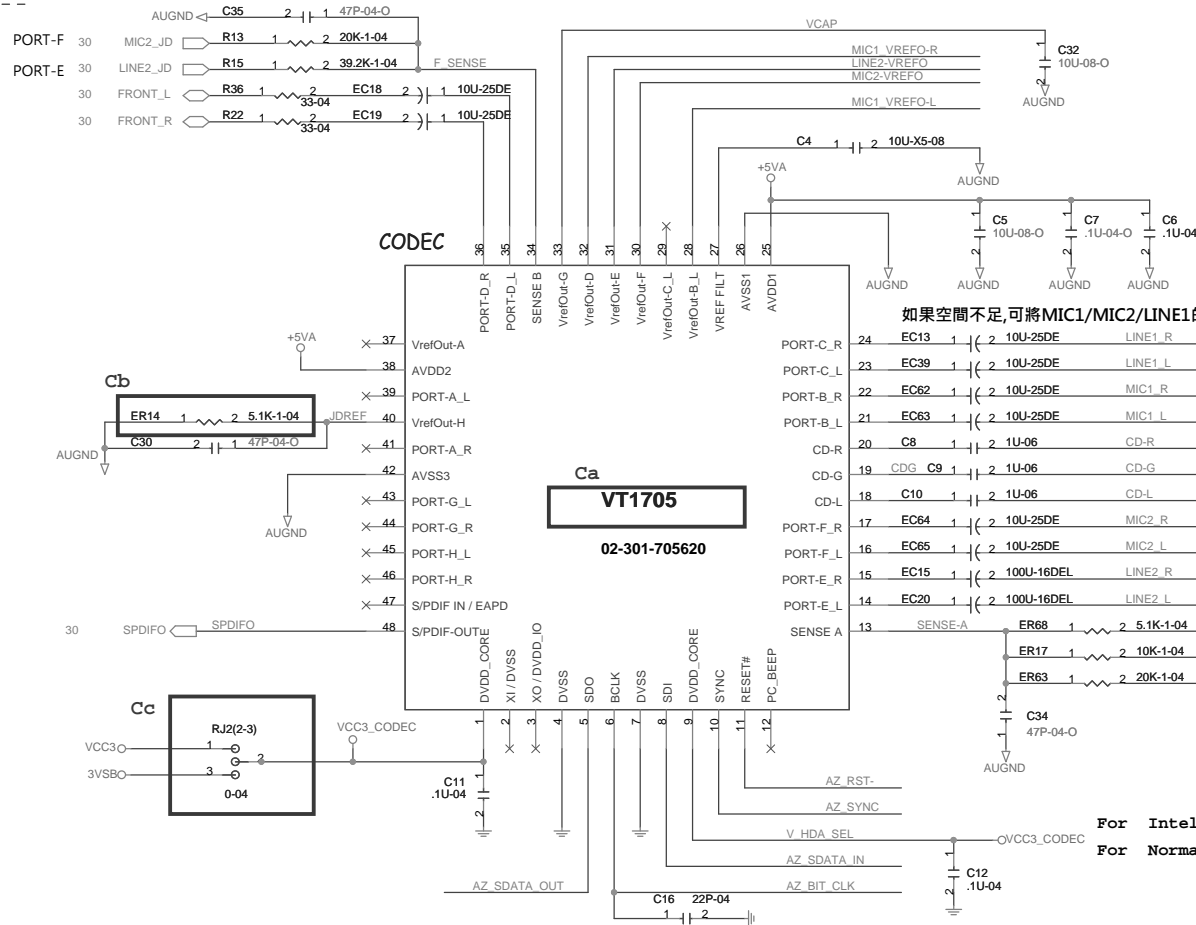
External Connection



MIC Bias



Cd



如果空間不足,可將MIC1/MIC2/LINE1的電容改10U-X5R-08

BOM Difference

Location	ALC662	VT1705
Ca	ALC662-VC-GRS	VT1705
Cb	20K-1-04	5.1K-1-04
Cc	ARJ2(1-2)	ARJ2(2-3)
Cd	2.2K-04	3.3K-04
Ce	75-04	16-04

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

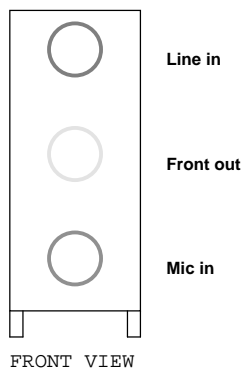
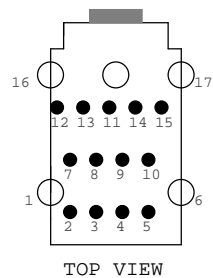
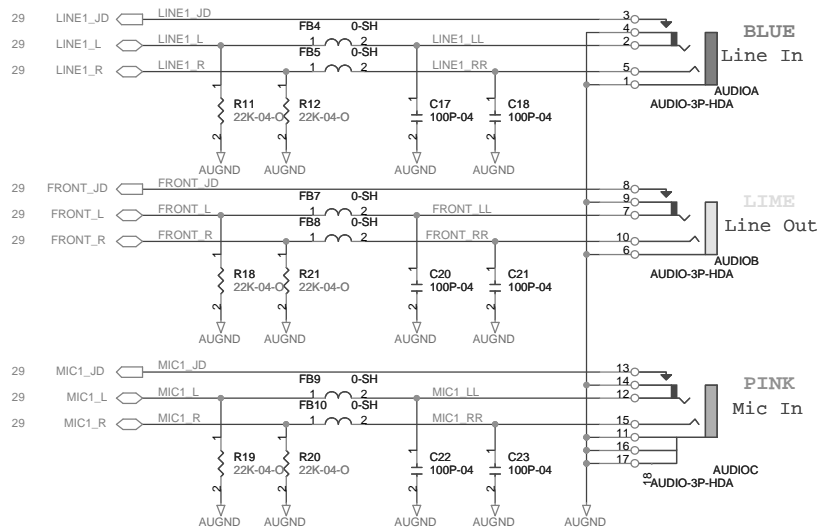
For Intel G4X HDMI support : 1.5V (pin1-2)
For Normal link : 3.3V (pin2-3)

External Connection

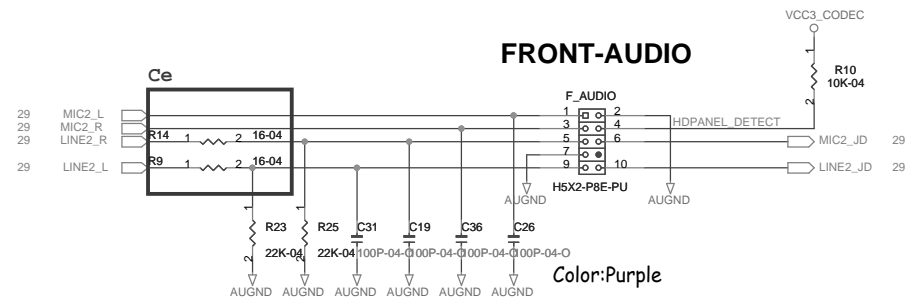
23 HDPANEL_DETECT  HDPANEL_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

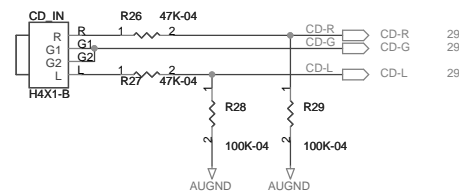
REAR-AUDIO



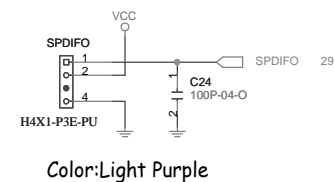
FRONT-AUDIO

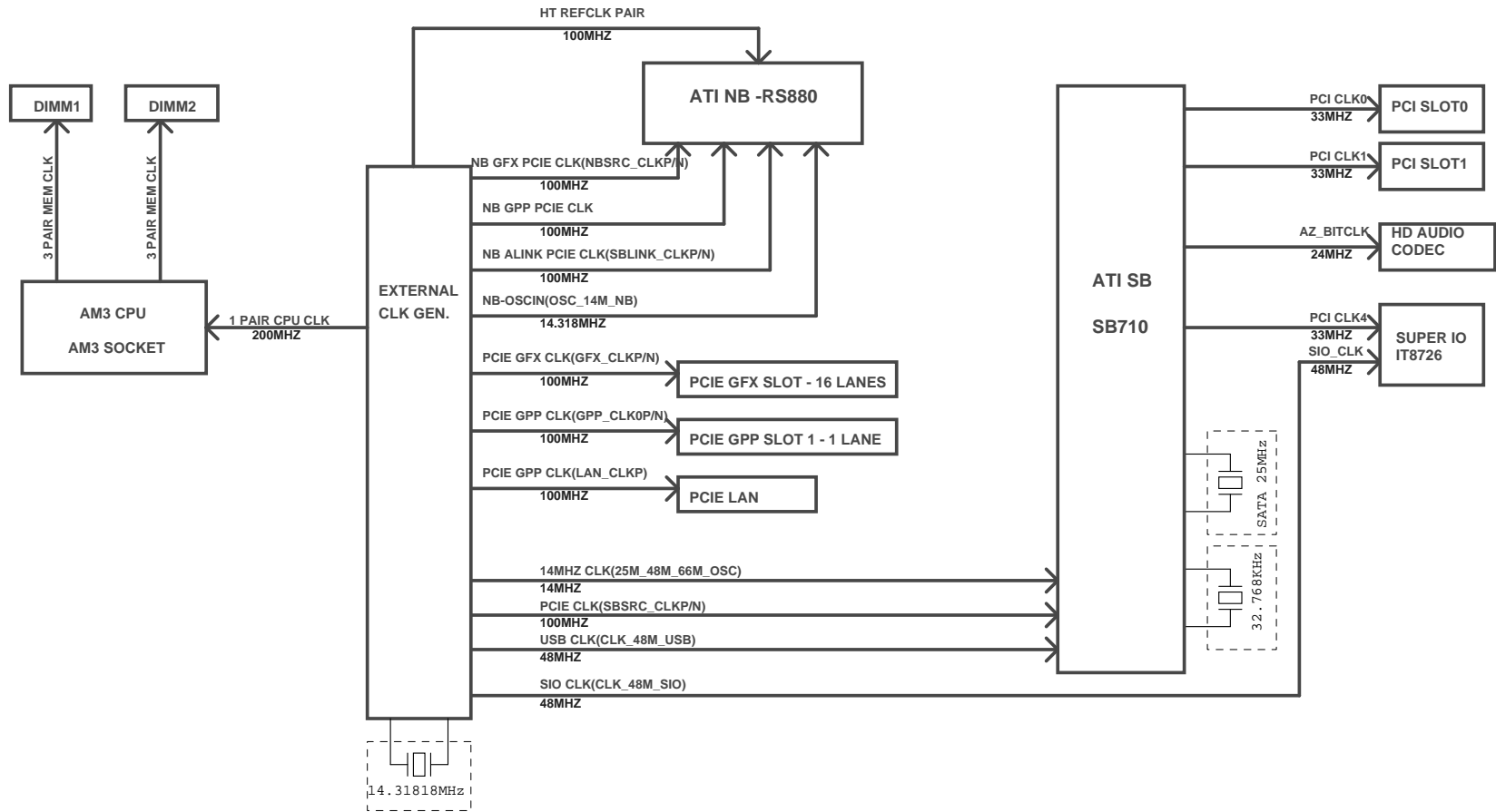


CD_IN



SPDIF-OUT





Power Sequence

